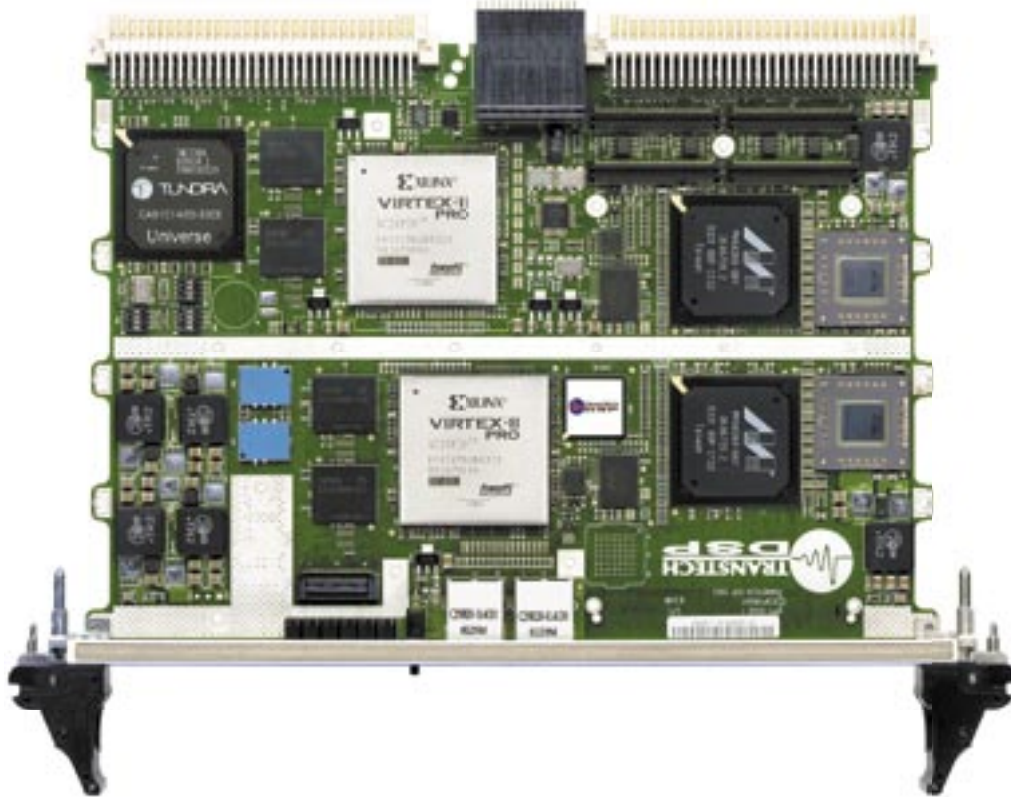


VPF1

Dual PowerPC, Dual Xilinx Virtex-II Pro FPGA Processing Engine



Features

- 2x PowerPC 7447 CPU nodes
- 2x Xilinx Virtex-II Pro FPGA nodes
- 8x 2.0-3.125Gbit/sec serial I/O links
- VME/VITA 41 VXS Compliant
- PMC site for local I/O
- Gbit Ethernet, RS232, RS422
- VxWorks, Linux, Gecade operating systems
- Embedded FPGA processing cores
- Rugged Roadmap



The VPF1 is a modular signal and data processing engine and a member of the Phoenix family of products. Phoenix products couple the power of the latest generation PowerPC CPUs, large Xilinx FPGAs and high-bandwidth multi-channel serial communication fabric. This creates a balanced and scalable compute platform for radar, sonar, electronic warfare and real-time imaging applications.

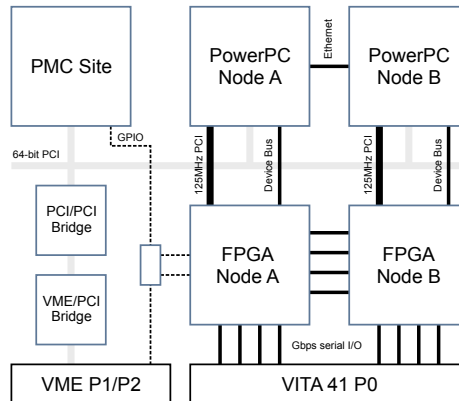
A complete rugged and systems based roadmap, with 6U and 3U variants, means that the VPF1 can be used as a common building block to a range of systems and results in accelerated development cycles and fast time-to-market.



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Overview

Architecturally, the VPF1 comprises of four processor nodes; two nodes are based on the PowerPC 7447 CPU and two nodes are based on Xilinx Virtex-II Pro FPGAs. All processor nodes have a fully distributed memory structure with multiple inter-node communications channels. The communications fabric hooks boards together as well as local processor elements for a scalable solution. The VPF1 is a VXS compliant board and able to handle Gbps communications. The VPF1 can also be provided as a VME64 board (requires VME Ext for power).



VPF1 Overview

Benefits

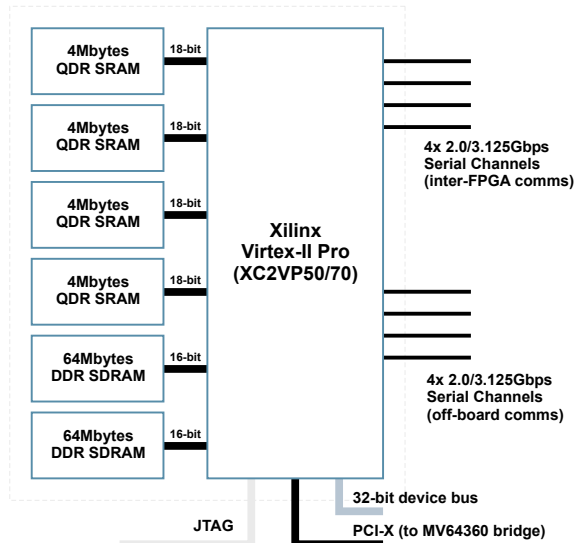
- PowerPC 7447 CPUs
 - Extensive code base
 - Wide support
 - High performance
- Virtex-II Pro FPGAs
 - No-compromise performance
 - Reduced bottlenecks when used for front-end processing
 - Wide range of IP cores
- VME/VXS Compliance
 - Access to wide range of VME I/O including, digital receivers, analog I/O and graphics
 - Access to high-bandwidth connections using VXS
- VxWorks, Linux, Gedae environments (call for availability)
 - Optimal tools for given applications
 - Heterogeneous development option (Gedae)
- Support software (libraries, drivers, utilities, examples) (call for availability)
 - Simplified code development
 - Optimal performance
 - Accelerated time-to-market
- Systems integration service
 - Free up engineering time
 - Access to signal processing hardware specialists

FPGA Processor Nodes

Xilinx Virtex-II Pro FPGA

The VPF1's FPGA nodes use Xilinx Virtex-II Pro devices with a choice of XC2VP50 or XC2VP70 variants.

- Eight 2.0/3.125Gbps SERDES transceiver pairs
- 64-bit/125MHz parallel bus to PowerPC bridge
- Four banks of 2M x 18-bit QDR SRAMs
- Two banks of 64Mbytes DDR SDRAM
- JTAG port



VPF1 FPGA Node

Gigabit Communication Channels

The Virtex-II Pro FPGAs feature 2.0/3.125Gbps RocketIO™ transceivers which provide fast communications between VPF1 compliant boards and between the VPF1's FPGAs: four RocketIO channels connect the two FPGA nodes and four channels from each FPGA are available for off-board communications. Each RocketIO channel has separate 8/10B encoded LVDS pairs for receive and transmit signals. Groups of RocketIOs from a single device can be 'bonded' together to synthesize fewer, but higher bandwidth data links if required. The raw low level data rates associated with 2.0/3.125Gbps datalinks are approximately 200/312.5Mbytes/sec in each direction per channel. The ability of the FPGA to generate 2.0 or 3.125Gbps datastreams is dependent on the speed grade of the FPGA. This is a build option.

Serial RapidIO, Infiniband and beyond

The VPF1's high-speed serial communications has been designed to be compatible with emerging standards and specifications (such as VITA 41 VXS) to address switch packet interfaces. The VPF1's serial channels are electrically compliant with Serial RapidIO, Infiniband and other serial interfaces. When FPGA IP cores are released, the VPF1 will accordingly be able to support these system fabrics.

QDR Memory Banks

Each VPF1 FPGA node includes four banks of 2Mx 18-bit QDR SRAM. QDR memory has the ability to perform read and write operations simultaneously. There are separate read and write busses, both of which clock data on both the rising and falling edge of the clock signal. The QDR memory is clocked at 125MHz for a read or write bandwidth of up to 500Mbytes/s per device. Read and write transfers can take place concurrently.

The QDR SRAM memory devices are directly linked and controlled by the FPGAs. This means that each QDR memory banks is not restricted in how it can be used and can be used to synthesize FIFO, linear addressable memory pools, bit-reversed addressing or circular buffers as best suits the application. Fast banks of SRAM are ideal for lookup tables, local data buffers and DSP operations such as dealing with concurrent (MAC) Multiply- ACcumulate data streams.

SDRAM Memory Banks

Bulk data storage buffering for the FPGA nodes can be provided through the dual 64Mbyte SDRAM banks. These can be used to store large data-sets such as image frames for medical imaging or temporal processing. Dual memory banks are also useful for decoupling I/O datastreams allowing data to be processed more easily while the other bank is filling up.

PowerPC Communications

In addition to Gigabit/sec serial communications, each FPGA has a fast data-link to one of the PowerPC node's PCI bridge (MV64360). This provides a 64-bit/125MHz PCI-X point-to-point link to the system PCI backbone and the PowerPC 7447's memory.

FPGA Configuration

Each VPF1 FPGA node's configuration is supplied by the attached PowerPC processor, with its configuration being stored in the PowerPC CPU's FLASH. Transtech supplies tools for programming the FPGA in both development and run-time environments. JTAG connectivity can also be used for FPGA configuration development.

An onboard battery (optional) is available so that encrypted keys can be stored for secure FPGA configurations.

FPGA IP Cores

The VPF1 can be provided with a range of IP cores including radar receivers, FFTs, FIR filters, QR processing and Floating-point arithmetic (add, multiple, divide, square-root). VHDL examples for SDRAM, QDR SRAM, DMA based data transfer and serial communications will also be available.

PowerPC Processor Nodes

Overview

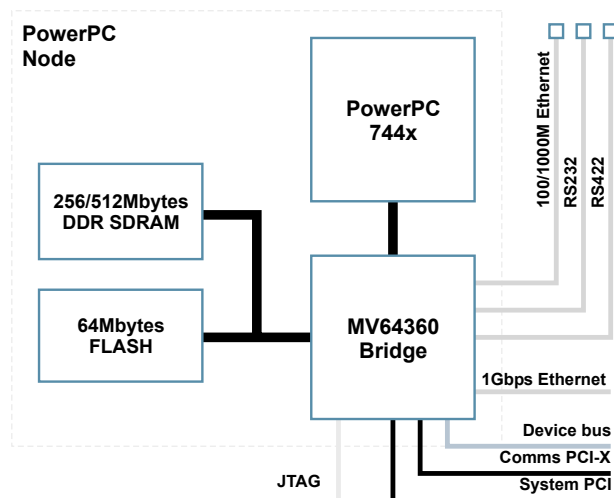
Each VPF1 includes two complete PowerPC 7447 compute subsystems complete with SDRAM, FLASH, Ethernet, serial I/O ports, fast PCI interfaces and operating systems support.

PowerPC 7447

The PowerPC 7447 is a new generation PowerPC processor offering both 1GHz+ performance, large onchip L2 cache (512Kbytes) and AltiVec unit - all within a low power implementation.

The VPF1 provides each PowerPC 7447 node with either 256 or 512Mbytes of DDR SDRAM (with ECC) per PowerPC node coupled via a Marvell MV64360 bridge and 32 or 64Mbytes FLASH memory. The SDRAM is implemented with 72-bit datapaths and clocked at 125MHz for an effective data rate of up to 2Gbytes/sec.

A highly integrated device the MV64360 provides two Gigabit Ethernet channels, RS422s and RS232 ports as well as a PCI and PCI-X interface.



VPF1 PowerPC Node

Ethernet

Two off-board Ethernet interfaces are provided, one from each PowerPC processor node. A further 1Gigabit Ethernet port link the two PowerPC nodes together. Each off-board port provides 10/100/1000Mbit (auto-negotiation interface) channels. The off-board interfaces are routed to the VME P2 connector and a build option provides front panel connectors for non conduction-cooled variants.

RS422 & RS232 Interfaces

One RS422 interface with RTS/CTS handshaking and one RS232 port is provided per PowerPC node. These ports are made available to the P2 connector (optionally via a VME P2 adapter/breakout module). Both ports are fully available for user applications and either can be used for a serial console as required by VxWorks for boot configuration.

Watchdog Timer

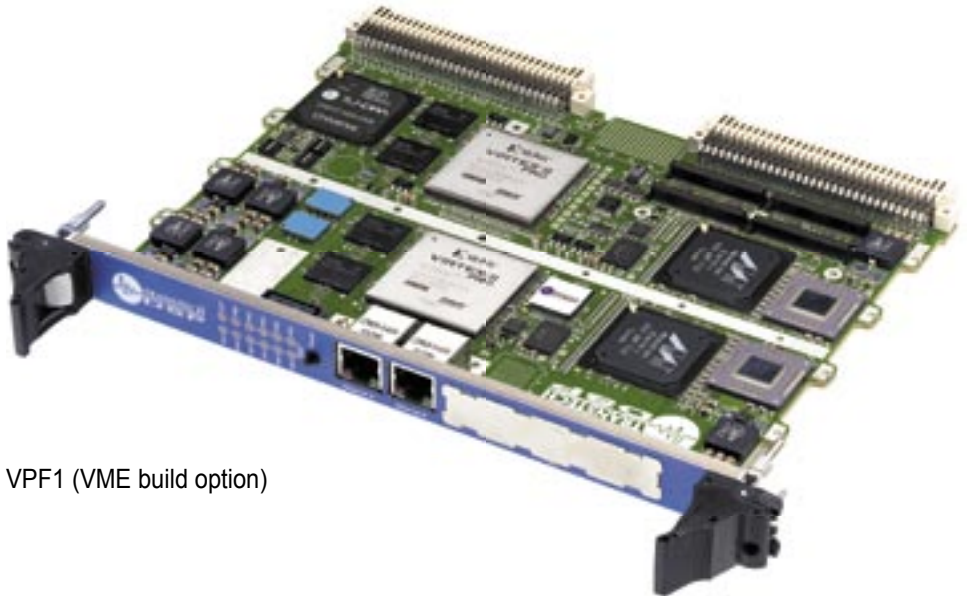
A hardware watchdog is provided (part of MV64360). This can be used to cause the board to reset and/or activate the NMI if the watchdog isn't serviced within a pre-defined period due to application failure.

Temperature and Power Monitors

Accessible via the PowerPC processor, the VPF1 includes two temperature sensors (controlled via an I²C bus) to monitor the temperature of the board and the FPGAs. The temperature sensors also have ADC capability. These are used to monitor the local supply voltages.

JTAG Interface

The VPF1 features multiple, independent JTAG chains via Firecron JTS01/JTS06 controllers and are accessible via both JTAG headers and the VME P2 connector. These connections also provide connectivity for the COP (PowerPC) and ChipScope/Agilent trace ports (FPGA) ports. The separate JTAG chains permit the board to undergo dynamic diagnostic during normal application run-time.



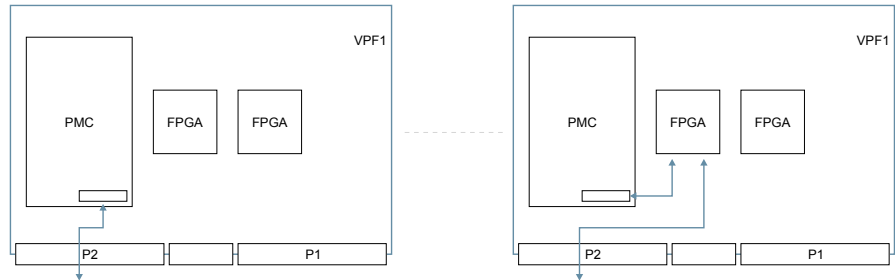
VPF1 (VME build option)

Input/Output

PMC Site & FPGA Parallel I/O

The usual I/O data stream for the VPF1 will be via the high-speed Gbps serial interfaces. However, the VPF1 also provides a 64-bit/66MHz PMC for local I/O such as analog I/O or frame grabbers. The PMC site has a PMC user I/O connector routed to the VME P2 connector (build option) for backplane communications.

As an alternative to PMC based backplane I/O, the VPF1 can use direct FPGA to VME P2 (rows a & c) linked I/O. FPGA backplane I/O and PMC backplane user I/O define the same connector pins and are mutually exclusive, but the VPF1 can have build options to range from PMC I/O only to FPGA I/O only or any sub-set in between (based on block of four signals) to use the VME P2 I/O.



PMC or FPGA Parallel I/O via VME P2

Backplane I/O Adapter

The majority of input/output for the VPF1 is available via the backplane: the system I/O (such as Ethernet and RS232) is routed to the VME P2 connector (rows z & d) and the high-speed serial I/O is routed to a P0 connector. To access the VME P2 based system I/O, Transtech can provide a breakout module. For conduction-cooled variants, the application backplane can incorporate these signals directly for a robust configuration.



Backplane I/O adaptor module

Backplane I/O

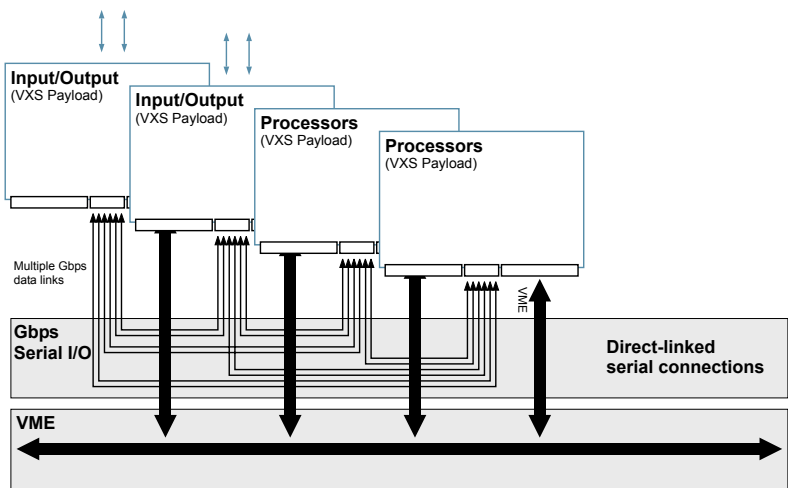
Each VPF1 has eight, off-board, multi-Gbps transceivers, each of which can be used to establish a point-to-point data link. These links can be wired to create a wide range of topologies to best suite the application such as pipelines of arrays to smoothly scale the system.

If more than eight datalinks are needed, then active switches can be used. These can be implemented within a custom backplane or (as defined in the VITA 41 VXS initiative) route all the passive signals to a switch card.

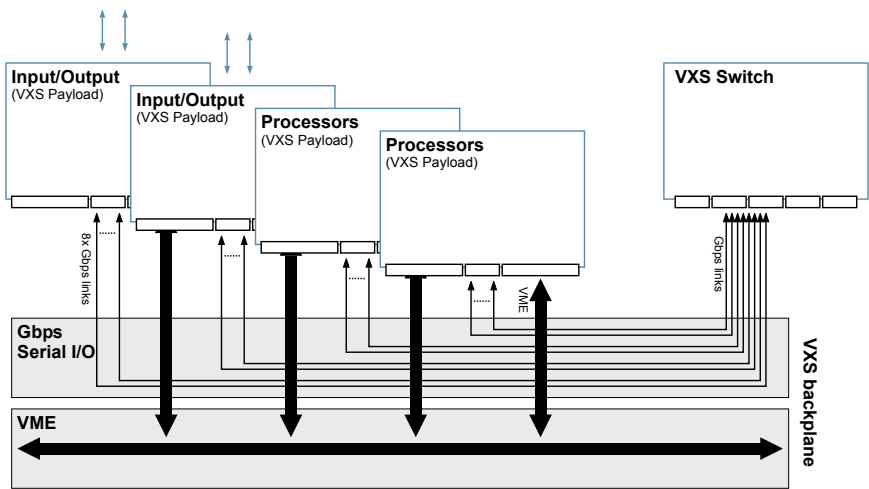
In order to achieve the Gigabit speeds data links, the P0 connector is a MultiGig (RT2) type connector with balanced differential signal routing and ground planes. This connector (as outlined in the emerging VITA 41 specification) is not compatible with the standard VME P0 connector which is not capable of handling the necessary bandwidth.

VXS backplanes are based on the VME bus backplane with an alternative P0 connector designed to support Gbps differential serial communications. Without this alternative P0 connector, a VXS card is a VME board that can be plugged into any VME backplane or system. The VITA 41 VXS specification defines a standard P0 pin-out for the payload cards that is fabric independent. Sub-VXS specifications define support for serial fabrics such as serial RapidIO, Infiniband, etc. In addition to the

payload cards, the VITA 41 VXS specification provides for switch cards (usually active) to control the routing of signal between the Gbps data links. For VXS backplanes that support this feature, a special switch slot is set aside in the backplane. VXS backplanes with switch slots provide a greater level of connectivity at the expense of an additional card slot. VXS backplanes can define a hardwired backplane interconnect to reflect different routing topologies such as pipelines and meshes.



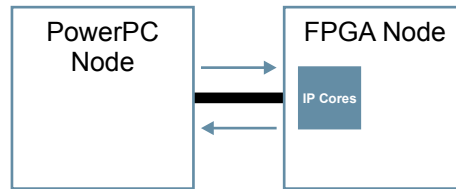
Fully connected VXS Cards via point-to-point data links using a hardwired (direct) switchless backplane



Fully connected VXS Cards with a Switch Card to Define the Data Link Routing

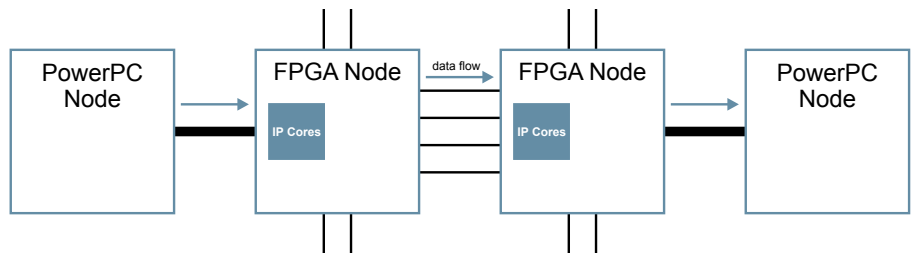
Using FPGA IP Cores and Communications

The communications architecture of the VPF1 means that the FPGAs can be used in a number of different ways: as co-processors, data processing pipelines or pure I/O. The FPGAs on the VPF1 can also be configured with the user's own FPGA code or be integrated with a wide range of third party IP cores.



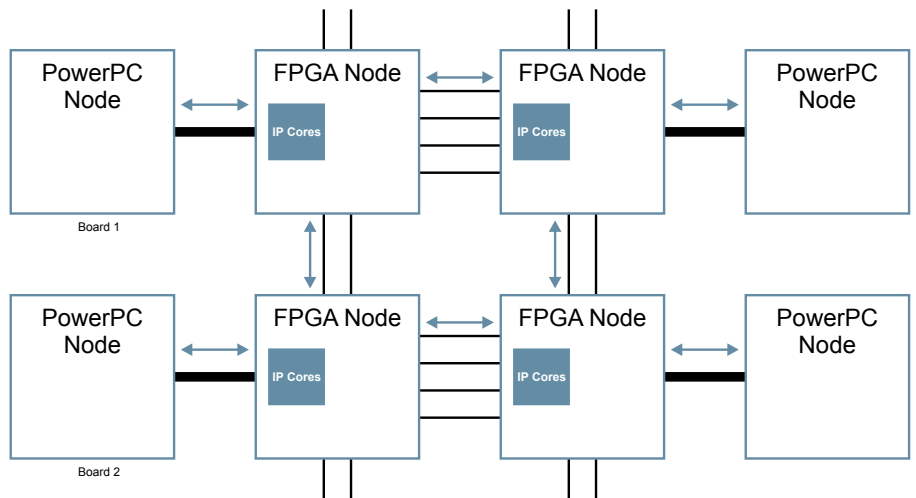
FPGA co-processor

The VPF1 employs a high-speed data link between each PowerPC CPU and one of the FPGAs. This allows the FPGA to be used as a co-processor: data is DMA'ed to the FPGA when one or more IP cores performs a compute intensive function such as FFTs, correlations or imaging warping and the resulting data is returned.



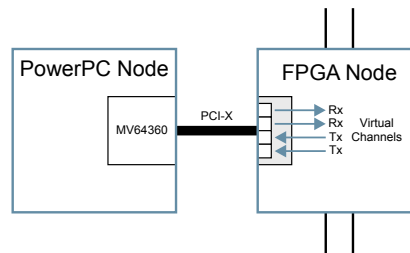
FPGA pipeline

As an alternative to a co-processor type model, the VPF1 can be used in a classic DSP pipeline arrangement. This is because the VPF1 has multiple data I/O paths which permit sustained data transfer without hitting data bottlenecks.



Multi-VPF1 Array

The VPF1's multiple datalinks are also available for off-board communications. These allow larger dataprocessing structures such as two or three dimensional arrays.



Virtual communications channels within an FPGA node

Each FPGA has a single 64-bit/125MHz datalink to a PowerPC node. This is a high-bandwidth data-link, but to make communications easier to IP cores, the VPF1 has firmware to establish a number of independent data paths within the FPGA that interface to the 64-bit link. These are virtual datachannels and make applications easier to develop. The VPF1 includes a combination of software libraries (APIs) and FPGA example firmware to show how the virtual data channels might be used.



Software Support

The VPF1 lends itself to different applications and markets. These demands require the VPF1 to be available with different layers of software support. For system critical applications, Built-In Test (BIT) provides a power up and run-time system diagnostic. To make application development easier I/O board drivers and optimized libraries will be available. The initial operating systems for VPF1 will include Linux, VxWorks and Gedae.

VxWorks (PowerPC)

VxWorks® is an industry standard real-time operating system and is the run-time component of the Tornado® II embedded development platform. Tornado II includes a comprehensive suite of cross-development tools & utilities and a full range of communications options from the host connection to the target. The microkernel supports a full range of real-time features, including fast multitasking, interrupt support, and both preemptive and roundrobin scheduling. The microkernel is designed to minimize system overhead and so enable fast, deterministic response to external events. The developer has many features available in the design of applications including using shared memory (for simple sharing of data), message queues, semaphores, events and pipes (for intertask messaging within a CPU), sockets and remote procedure calls (for network-transparent communication), and signals (for exception handling).

Gedae (PowerPC and FPGA)

Gedae is a software development environment based on a block diagram programming paradigm (CASE tool): through the use of block diagrams, functionality is specified and Gedae implements the application by generating code targeted to specific embedded hardware. Gedae is a heterogeneous environment and has support for processors including the PowerPC CPU, FPGAs and TigerSHARC DSP. This makes a Gedae application easily portable thereby retaining valuable code for future upgrades.

The Gedae toolset is comprised of a workstation development environment and target-specific runtime kernels for embedded targets.

Included in Gedae are a variety of tools to support the mapping of applications to multiple processors, autogeneration of the code to run on those processors and visualization of both individual and multiprocessor execution activity.

Gedae provides intuitive interfaces for:

- Designing data flow
- Controlling implementation
- Observing functionality, implementation, and performance
- Generating a stand-alone application

Gedae has its own easy-to-understand language: The block diagram graphical language, used to express the application algorithms. Various graphical displays, such as scopes and constellation diagrams, can be used to analyze and verify constructed algorithms. Once the algorithm's behavior is verified, the implementation is specified and the performance is optimized.

Gedae's intuitive design environment inherits the power of the C programming language. Boxes modularize C-code and encapsulate any of the following behavior:

- **Application Control**
Dynamic behavior can be incorporated into a box, making application control possible.
- **Interface with Input/Output**
I/O devices can be interfaced through Gedae function boxes so that graphs can do real time data processing.
- **Graphical User Interfaces (GUIs)**

A box library is included with Gedae, so users can design GUIs as block diagrams.

- **Dynamic Load Balancing and Fault Tolerance**

Boxes with dynamic inputs and outputs allow graphs to be constructed with load balancing and fault tolerance.

- **Interface with MATLAB**

A box library is included with Gedae so that users can interface the libraries and displays of MATLAB in their Gedae graphs.

FPGA Communications Library

To allow the FPGA to be configured by a host, Transtech supplies loader utilities for VxWorks and Linux hosts. This enables developers to use their standard tools then to transfer the application to the VPF1 easily and quickly. A host based FLASH programming utility is provided so that the FPGA is automatically configured on power-up without the need of the host.

Host Tools

Software development is supported using the usual compilers for the operating system platform. This is Microsoft Visual C++ for Microsoft platforms and the GNU compiler for VxWorks, Linux and LynxOS. The BSP library provides integration support for using the VPF1 from within a host application. It is a C++ library supporting general hardware access and the implementation of high-speed DMA routines. Full source code for the libraries and examples are supplied including continuous mode DMAs.

The host services provided by the libraries usually requires the support of an operating system dependent device driver. Drivers for VxWorks, Linux and Gedae operating systems will be supported. Host utilities are provided to give the user a graphical user interface with a complete view of the board hardware (registers, memory etc.).

VS IPL - PowerPC DSP Library

The VS IPL library provides a core set of common DSP functions for the VPF1 and optimized for the PowerPC 74xx (AltiVec) CPUs. The basis behind the DARPA definition is to provide a processor and operating-system independent set of DSP functions thereby allowing for maximum code portability.

- **VS IPL API**

Over 500 functions, DARPA sponsored, PowerPC G4 (AltiVec) optimizations

- **VS IPL features**

Portability, Object-based description, Opaque objects such as blocks, and views on the blocks (vectors, matrices, and tensors), Development and production modes, Public and private data arrays enabling implementation optimizations, Explicit memory/algorithm hints

- **Functionality**

Scalar Functions, Vector and Matrix (scalar, unary, binary, logical arithmetic, selection and data generation), Linear Algebra, Signal Processing (FFTs, window, filter and convolution routines), Image Processing

Power-On Self Test

The VPF1 can be configured to go into a self-test mode at powerup. The built-in test runs from FLASH memory prior to any operating system kernel being started. All the major system components are checked to see if they are operational with the diagnostic results written to registers. If the board fails, these results can be retrieved using a debugger/emulator tool to determine where the failure occurred. Some of these tests include

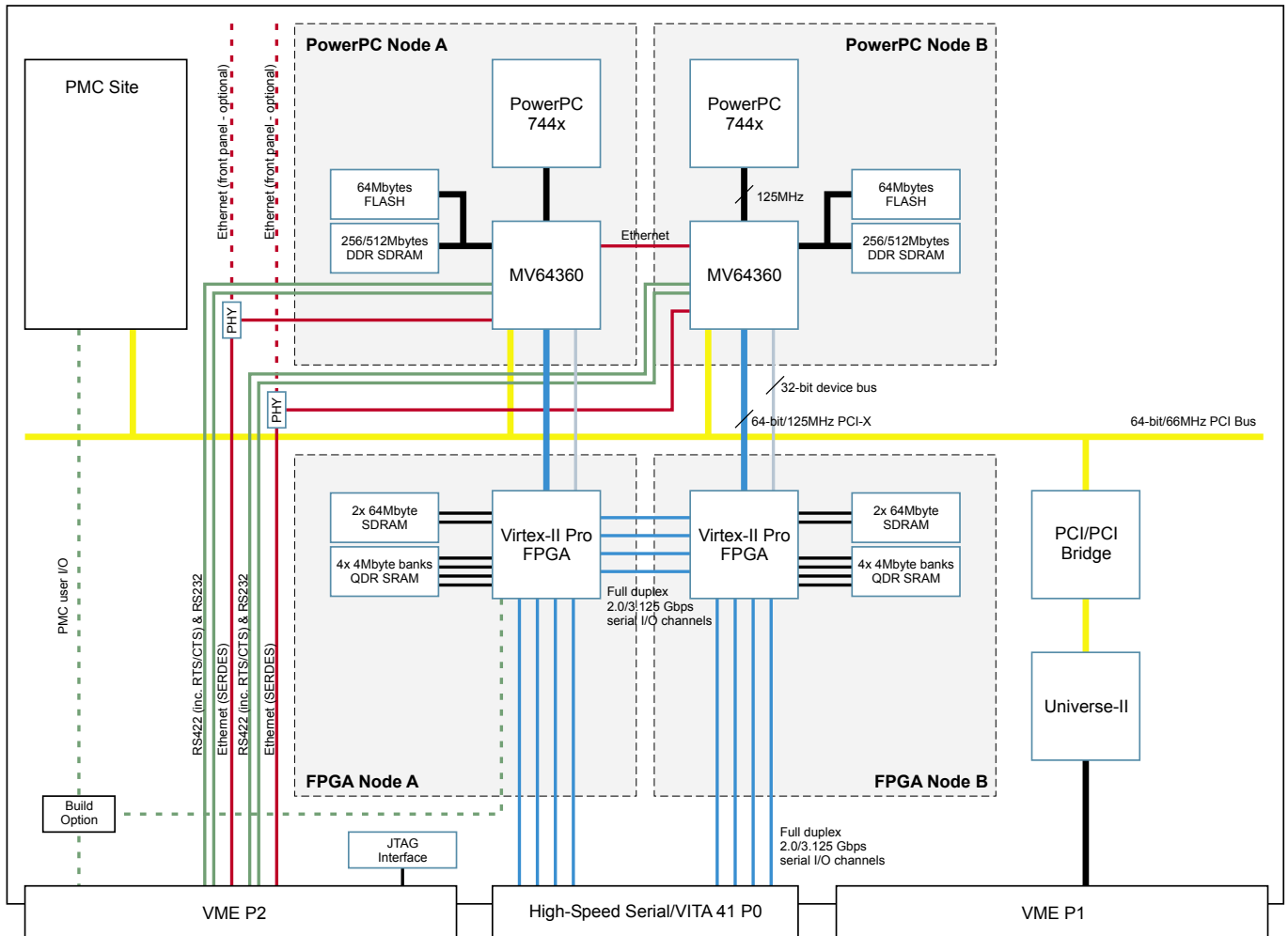
The VPF1 can also be tested or run diagnostic functions when running applications under VxWorks or Linux. These are accessed using the 'board test library'. Some of these tests are destructive; for example the memory test will destroy the contents of the memory tested.

Ruggedization Levels

Ruggedization	Level 1 (L1)	Level 2 (L2)*	Level 4 (L4)*
Cooling	Air/Convection	Air/Convection	Conduction
Temperature			
Operating	0°C to 50°C	-10°C to 65°C	-40°C to 75°C
Storage	Inlet 4 cfm air flow at sea level -40°C to 85°C	Inlet 4 cfm air flow at sea level -40°C to 85°C	card edge temp -55°C to 85°C
Humidity			
Operating	0 to 95% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing
Storage	0 to 95% non-condensing	0 to 100% non-condensing	0 to 100% non-condensing
Vibration			
Sine	na	na	10 g peak (15-2 kHz)
Random	na	0.02 g ² /Hz (20 to 2000 Hz)	0.1 g ² /Hz (15-2 kHz)
Shock	na	30 g peak (half sine 11ms)	40 g peak (half sine 11ms)
Conformal Coat	No	Yes	Yes

* Subject to qualification

Block Diagram



Specification

PowerPC Nodes

Number	2
Processor (per node)	PowerPC 7447A (600MHz-1GHz)
FLASH (per node)	32 or 64Mbytes
Bridge (per node)	Marvell MV64360
SDRAM (per node)	256 or 512Mbytes
FLASH (per node)	32/64Mbytes
Ethernet (per node)	10/100Mbps (or 1Gbps)
Serial I/O (per node)	1x RS232, 1x RS422 (with RTS/CTS)

FPGA Nodes

FPGA	XC2VP50 or XC2VP70
Rocket IO Speed	2.0Gbps (-5 speed grade) 3.125Gbps (-6 speed grade)
SDRAM	128Mbytes (with ECC)
QDR SRAM	4 banks 2 or 4Mbytes per bank 18-bit data paths

Inter-Node Communications

FPGA to FPGA	4x 2.0/3.125Gbps
PowerPC to FPGA	64-bit/100MHz link
PowerPC to PowerPC	1Gbps Ethernet
Other	Shared 64-bit/33MHz PCI

Off-board Communications

High-Speed Serial	8x 2.0Gbps (4 per FPGA node) MultiGig (VITA 41 style) Connector
VME	VME64 (Universe II Bridge)
Other	Direct FPGA (VME P2) connections (build option)

Debugging

JTAG	Multiple JTAG/COP chains VME P2
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PMC

Number of Sites	1
I/O Routing	User I/O to VME P2 (build option)

Software Support

Operating Systems	VxWorks (PowerPC) Linux (PowerPC) Gedae (PowerPC + FPGA)
Libraries	Signal & Image Processing (PowerPC)
FPGA Cores	FFT, Floating-Point Arithmetic, QR Processing, Radar Receiver User Configurable
Other	Built-In Test (BIT)



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