

# SP/S4-AMC

## Altera Stratix® IV GX AdvancedMC with 4 SFP/SFP+



- High density Altera Stratix IV GX supported by BittWare's ATLANTiS FrameWork for FPGAs
- 4 SFP/SFP+ transceivers on front panel
- BittWare's FINE™ III Host/Control Bridge for control plane processing and host interface
- Up to 2 GBytes on-board memory
- I/O includes 10/100/1000 Ethernet, SerDes, LVDS, RS-232, and JTAG

**B**ased on Altera's Stratix IV GX FPGA, BittWare's SP/S4-AMC (SP/S4AM) is a full-size, single wide AdvancedMC that can be attached to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The SP/S4AM features a high-density, low-power Altera Stratix IV GX FPGA designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable AMC. BittWare's ATLANTiS FrameWork, in conjunction with the FINE III Host/Control Bridge, greatly simplifies application development and integration of this powerful board. Four small form-factor pluggable-plus (SFP/SFP+) compact optical transceiver connectors are available on the front panel. The board also provides an IPMI system management interface, a configurable 15-port AMC SerDes interface supporting a variety of protocols. The board also features 10/100/1000 Ethernet, two banks of DDR3 SDRAM, two banks of QDRII+ SRAM, and Flash memory for booting the FPGAs and FINE.

### SFP/SFP+ FPGA Mezzanine Card

The SP/S4AM provides a four-cage SFP/SFP+ connector on the front panel with each transceiver providing support for virtually any serial communication standard, including: Fibre Channel, GigE, SONET, CPRI, and OBSAI. The four SFP/SFP+ SerDes channels are connected directly to the Stratix IV GX FPGA.

### Altera Stratix IV GX FPGA

The Altera Stratix IV GX was specifically designed for serial I/O-based applications requiring high-density, reconfigurable logic. The Stratix IV GX provides 19 full-duplex, multi-gigabit transceivers, 16 of which are high-performance, supporting PCI

Express (Rev 1.0/2.0), 10 GigE, GigE, Serial RapidIO (Rev 1.0/2.0), and SerialLite II standards. It contains up to 530k equivalent LEs, over 20 Mbits of embedded memory, and 1,024 embedded 18x18 multipliers. The FPGA is supported by BittWare's ATLANTiS FrameWork for FPGA development and provides seamless routing of all on-board data, I/O, and memory.

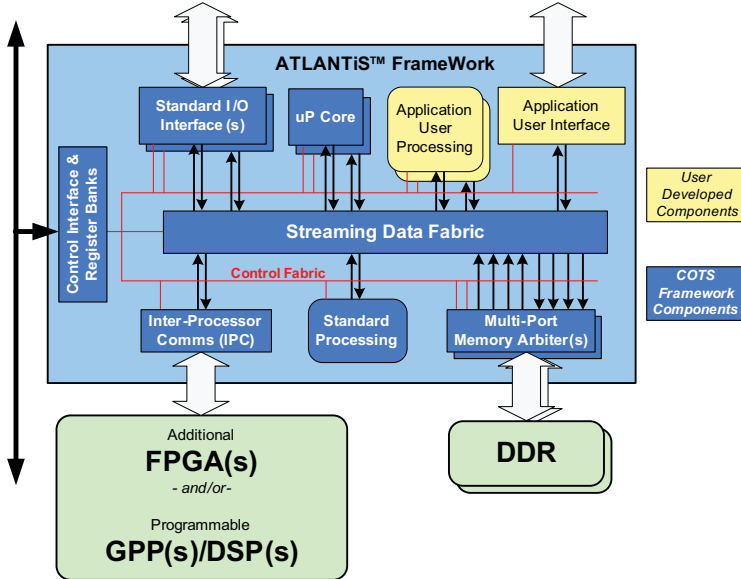
### Fat Pipes, Common Options, and I/O Interfaces

The Stratix IV GX FPGA interfaces to 3 ports (1, 2, & 3) in the AMC common options region, and 16 ports in the AMC fat pipes region (4 - 15, 17 - 20). These 19 ports provide a network data and control switch fabric interface on the AMC connector, with 12 supporting up to 6.25 GHz, 3 supporting up to 3.125 GHz, and the remaining 4 providing LVDS rear-panel I/O. All AMC clocks are also connected to the Stratix IV GX. The front panel provides 10/100 Ethernet, 2 RS-232 ports, and a JTAG port for debug support.

### ATLANTiS™ FrameWork

BittWare's ATLANTiS FrameWork for FPGA development (see Figure 1) provides reconfigurable FPGA components, along with the infrastructure necessary to implement, simulate, synthesize, validate, and deploy a complete FPGA application on the Stratix IV GX. ATLANTiS FrameWork delivers fully validated FPGA physical interfaces for all board-level I/O and communications, including high-speed SerDes and external memory control, along with resource management components such as buffering, DMA engines, and arbitration. Each component can be easily monitored and controlled via an addressed path implemented using Altera's open standard Avalon Memory Mapped Interface. Similarly, Altera's open standard Avalon Streaming

Figure 1: ATLANTiS FrameWork Architecture Overview



Interface is used to implement point to point data transport between ATLANTiS components. A set of reconfigurable fabric components such as multiplexers, switches, decoders, and FIFOs expand the interconnect options for both memory mapped and streaming interfaces. ATLANTiS FrameWork removes the burden of reinventing low-level IP for the FPGA, thus freeing developers to focus on their unique value-added development.

### FINe™ III Host/Control Bridge

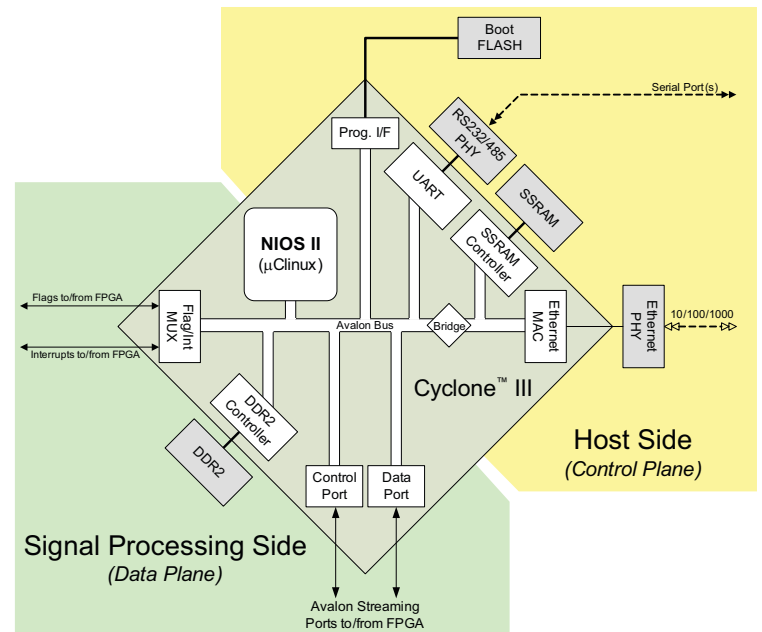
BittWare's FINe III Host/Control Bridge (see Figure 2) implements a complete control plane interface for the SP/S4AM, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. BittWare's BittWorks Toolkit provides extensive software support and is tightly integrated with the FINe.

The FINe III provides GigE via the common options region, along with 10/100 Ethernet and an RS-232 monitor port on the AMC front panel, and is connected to the FPGA via a local control bus.

### Development Tools

BittWare offers complete software support for the SP/S4AM with its BittWorks software tools. BittWorks is a suite of software development tools, designed to make developing and debugging applications for BittWare's signal processing boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely. The BittWorks software tools include host interface libraries, a wide variety of diagnostic utilities and configuration tools, debug tools, and I/O drivers, all of which are tightly integrated with the ATLANTiS FrameWork and the FINe.

Figure 2: FINe III Architecture Overview



## Specifications

### BOARD ARCHITECTURE

#### FPGA

- Altera® Stratix® IV GX FPGA (4SGX230/530)
- Supported by BittWare's ATLANTiS™ FrameWork
- 16 full-duplex, high-performance, multi-gigabit SerDes transceivers @ 6.25 GHz
- 3 full-duplex, multi-gigabit SerDes transceivers @ 3.125 GHz
- Over 530k equivalent LEs
- Over 20 Mbits of RAM
- Over 1,024 embedded multipliers

#### External Memory

- 2 banks of up to 1 GByte DDR3 SDRAM configured as x32
- 2 banks of up to 9 MBytes QDRII+ SRAM configured as x18
- 64 MBytes of Flash memory for booting FPGA and FINE

#### SFP/SFP+ FMC

- 4 SFP/SFP+ transceivers on front panel connected to FPGA via SerDes
- EEPROM available via I<sup>2</sup>C

#### Fat Pipes Interface

- 12 ports (4 - 11, 20 - 17) @ up to 6.25 GHz via ATLANTiS™ FrameWork, configurable to support PCI Express (Rev 1.0/2.0), Serial RapidIO (Rev 1.0/2.0), GigE, 10GigE/XAUI
- 4 ports (12 - 15) of LVDS I/O (4 In, 4 Out)

#### Common Options Interface

- BittWare's FINE™ III Host/Control Bridge providing GigE on port 0
- Ports 1, 2 & 3 via ATLANTiS™ FrameWork, configurable to support PCI Express, Serial RapidIO, and GigE

#### Other AMC Edge Connections

- All AMC clocks brought to ATLANTiS
- Module Management Control (MMC) Interface implementing IPMI for temperature monitoring and hot-swap support
- Connectorless footprint for Agilent / Tektronix logic analyzers

#### AMC Front Panel I/O

- 10/100 Ethernet to FINE
- RS-232 port to Stratix IV GX
- RS-232 port to FINE
- JTAG debug interface to the Stratix IV GX

#### Size

- AMC full-size, single width format compatible with AMC.0 specification R2.0

### DEVELOPMENT TOOLS

#### BitWorks Tools for Application Development

- BittWorks Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks Porting kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems
- BWIO - software library for controlling I/O on BittWare boards

#### FPGA and DSP Code Development

- Altera Quartus® II software

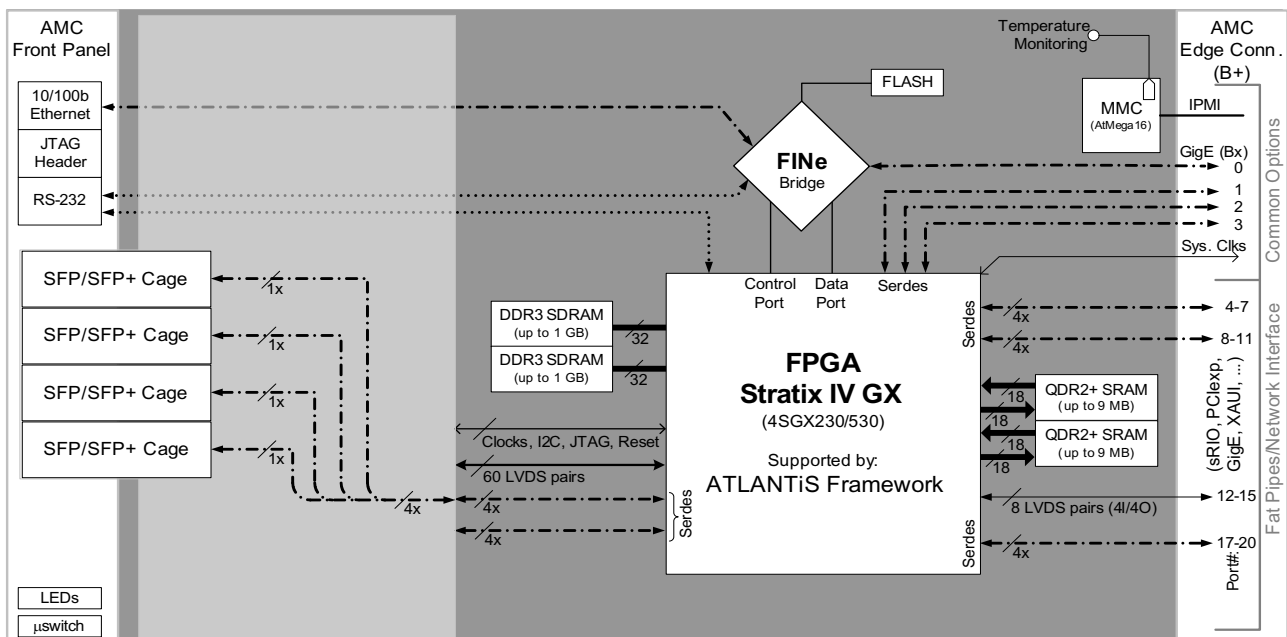
#### Development Platforms

- MicroTCA Rapid Development Platform

#### Accessory Boards

- BittWare GXBO breakout board for front panel I/O access

Figure 3: SP/S4AM System Block Diagram



## Ordering Options

SP/S4AM-RW-YY-Z-AABB-CDEFG-HHI							
RW	Ruggedization OU = Commercial (0C to 50C)*	YY	SFP Transceiver 00 = No transceiver (default)	Z	Front Panel Input Clock 0 = Not Installed* 1 = Installed†	AA	FPGA Size 23 = Altera Stratix IV GX 230* 53 = Altera Stratix IV GX 530†
BB	FPGA Speed Grade C2 = Commercial Speed Grade 2† C3 = Commercial Speed Grade 3* C4 = Commercial Speed Grade 4† I3 = Industrial Speed Grade 3† I4 = Industrial Speed Grade 4†	C	DDR3 Bank A Size 0 = None 7 = 256 MB† 8 = 512 MB* 9 = 1 GB†	D	DDR3 Bank B Size 0 = None 7 = 256 MB† 8 = 512 MB* 9 = 1 GB†	E	QDRII+ Bank A Size 0 = None* 2 = 9 MB
F	QDRII+ Bank B Size 0 = None* 2 = 9 MB	G	FiNe Flash Size 5 = 64 MB† 6 = 128 MB*	HH	Front Panel F3 = Full Size - SPFM Cutout	I	Front Panel SerDes Connector 0 = Not Populated

\* Default

† Contact BittWare for availability.

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