

S5-PCIe

Altera Stratix® V GX/GS PCIe Board with up to two VITA 57 FMC I/O Sites and Dual QSFP+



- High density Altera Stratix V GX/GS supported by BittWare ATLANTiS™ FrameWork for FPGAs
- Up to two VITA 57 FMC sites for processing and I/O expansion
- Two QSFP+ cages (optional)
- Up to 32 GB of DDR3 with ECC
- PCIe x8 interface supporting Gen 1, Gen2, or Gen3
- Utility I/O includes: USB 2.0, RS-232, and JTAG

BittWare's S5-PCIe (S5PE) is a PCIe x8 card based on the high-bandwidth, power-efficient Altera Stratix V GX or GS FPGA. Designed for high-end applications, the Stratix V provides a high level of system integration and flexibility for I/O, routing, and processing. When combined with BittWare's Anemone FPGA co-processor and the ATLANTiS FrameWork for FPGA integration, the S5PE creates a flexible and efficient solution for high-performance signal processing and data acquisition. The board provides up to 32 GB of DDR3 SDRAM with error-correcting codes (ECC). Providing additional flexibility are up to two VITA 57 FMC sites for enhancing the board's I/O and processing capabilities. The board also has the option of two front-panel QSFP+ cages for serial I/O.

Altera Stratix V GX/GS FPGA

The Altera Stratix V FPGA has been optimized for high-performance, high-bandwidth applications with integrated up to 14.1 Gbps transceivers supporting backplanes and optical modules. It supports 1.6 Tbps of serial switching capability, up to 1,755 GMACS of signal-processing performance, and 2 x72 DDR3 memory interfaces. The Stratix V also provides PCI Express x8 via a hard IP block and supports configuration by PCI Express using the existing PCI Express link in your application. For additional flexibility, the Stratix V supports transceiver and core reconfiguration on-the-fly while other portions of the

design are running. The FPGA implements BittWare's ATLANTiS FrameWork and provides seamless routing of all on-board data, I/O, and memory.

VITA 57 FMC Sites for Processing and I/O Expansion

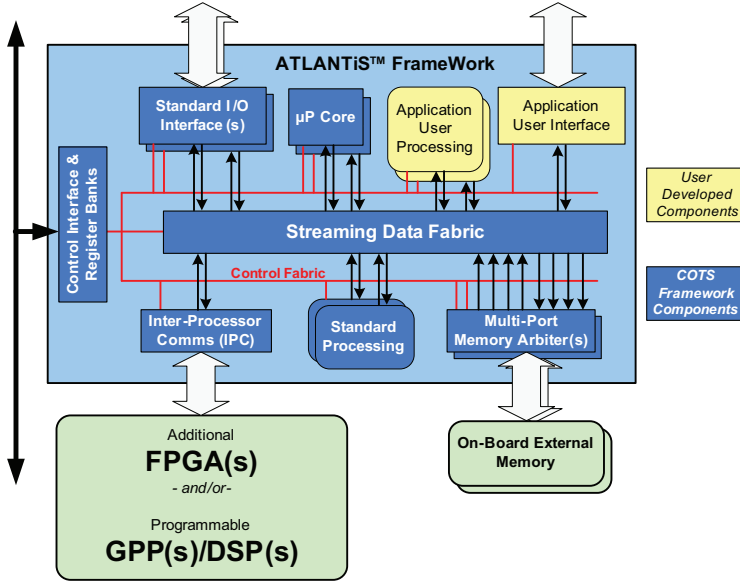
The S5PE features up to two FMC (FPGA Mezzanine Card) sites, which provide high-performance SerDes and LVDS, along with clocks, I²C, JTAG, and reset connected to the Stratix V. The sites are based on the VITA 57 mezzanine standard for FPGA I/O, enabling designers to customize the S5PE to their individual needs with optional FMC I/O boards.

I/O Interfaces

In addition to the FMC I/O, the S5PE provides a variety of interfaces for high-speed serial I/O as well as debug support. Two QSFP+ cages are optionally available on the front panel (in place of the front panel FMC interface), providing support for virtually any serial communication standard, including: Fibre Channel, 40 GigE, 10 GigE, SONET, CPRI, OBSAI, Serial RapidIO, and SerialLite. The eight QSFP+ SerDes channels are connected directly to the Stratix V FPGA.

The x8 PCIe interface provides 8 SerDes lanes to the Stratix V FPGA. USB 2.0, RS-232, and JTAG interfaces are available for debug and programming support.

Figure 1: ATLANTiS FrameWork Architecture Overview



ATLANTiS FrameWork: Simplified FPGA Development

While FPGAs provide significant performance benefits, the FPGA development process can be both time-consuming and difficult. BittWare's **ATLANTiS Framework** (AFW) addresses these limitations by providing infrastructure that supports FPGA development at a higher abstraction level. AFW provides reconfigurable FPGA components and the necessary infrastructure to implement, simulate, synthesize, validate, and deploy a complete FPGA application on BittWare's Altera-based FPGA products.

ATLANTiS FrameWork simplifies development by providing streaming and memory mapped interconnect fabrics, low-level physical interfaces and timing constraints, and pre-existing projects and I/O configuration so that users do not have to start from scratch. Its Avalon common interface components are reusable and portable; and a standard component structure, reconfigurable HDL components, and supporting software development libraries promote design portability and FPGA code reuse. AFW also allows for improved design exploration and validation with standardized simulation and test resources and with its support for flexible, static, and run-time reconfiguration. By providing the entire standard infrastructure that supports FPGA development, AFW removes the burden of reinventing low-level IP for the FPGA, thus freeing developers to focus on unique value-added development.

Anemone: Floating Point Co-Processor for FPGA

Anemone is a truly C-programmable floating point compute engine that achieves superior power efficiency and processing performance by working alongside an FPGA as a co-processor. The FPGA handles all the memory, I/O interfacing, protocol processing, and special functions, in addition to any computational tasks it may perform. This leaves the Anemone free to efficiently perform complex processing tasks.

Anemone enables partitioning of processing between software and hardware, and reduces system development cost by enabling out-of-the-box execution of applications written in regular ANSI-C. Ideal for implementing complex algorithms and for implementing processing with changing requirements, Anemone is a low risk and low power way to add processing resources. Anemone is available for the S5PE on a quad-processor VITA 57 FMC.

Development Tools

BittWare offers complete software support for the S5PE with its BittWorks II software tools. BittWorks II is a suite of software development tools, designed to make developing and debugging applications for BittWare's signal processing boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely. The BittWorks software tools include host interface libraries, a variety of diagnostic utilities and configuration tools, debug tools, and I/O drivers, all of which are tightly integrated with the ATLANTiS FrameWork.

S5PE Specifications

BOARD SPECIFICATIONS

FPGA

- Altera® Stratix® V GX/GS FPGA
- Supported by BittWare's ATLANTiS™ FrameWork
- 26 full-duplex, high-performance, multi-gigabit SerDes transceivers @ up to 14.1 GHz
- More than 1 million logic elements (LEs) available
- Up to 50 Mb of embedded memory
- 1.4 Gbps LVDS performance
- Up to 3,510 variable-precision DSP blocks
- Embedded HardCopy Blocks

External Memory

- Two banks of up to 16 GByte DDR3 SDRAM x 72 with ECC
- 128 MBytes of Flash memory for booting FPGA

PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

USB Header

- USB 2.0 interface for debug and programming

Debug Utility Header

- RS-232 port to Stratix V
- JTAG debug interface to Stratix V

QSFP+ Cages (optional)

- 2 QSFP+ cages on front panel connected to FPGA via 8 SerDes

VITA 57 FMC Site A (optional)

- 10x high-performance SerDes
- 80 LVDS
- Clocks, I²C, JTAG, and reset

VITA 57 FMC Site B

- 48 LVDS
- Clocks, I²C, JTAG, and reset

Size

- Full-length, standard-height PCIe slot card

VALUE-ADD PRODUCTS FOR FPGA

Anemone FPGA Co-Processor

- C-programmable floating point co-processor for FPGAs
- 1 GHz multicore processor
- 32 GFLOPS in ~ 2 Watt total chip power
- Available for the S5PE on a quad-processor VITA-57 FMC

ATLANTiS FrameWork

- FPGA FrameWork for Stratix V GX/GS
- Reconfigurable HDL components
- Low-level physical interfaces and timing constraints
- Supporting software libraries
- Example and template projects
- Standardized simulation and test resources

DEVELOPMENT TOOLS

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks II Porting Kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems
- BWIO - software library for controlling I/O on BittWare boards

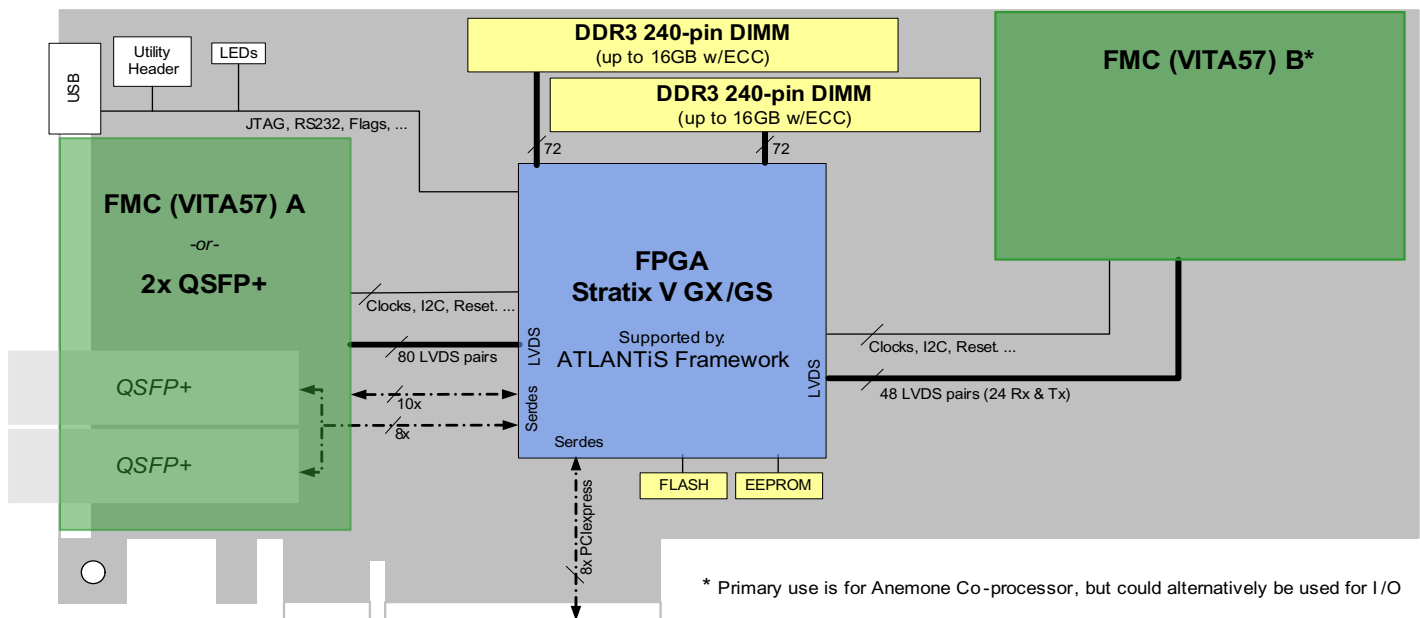
FPGA Development

- ATLANTiS FrameWork
- Altera Quartus® II software

Accessory Boards

- BittWare GXBO breakout board for front panel I/O access

Figure 2: S5PE System Block Diagram



S5PE Ordering Options

S5PE-RW-AABCCDEE-FFGG-HIJ					
RW	Ruggedization 0U = Commercial (0C to 50 C)*	AA	Altera Stratix V FPGA Family GX = Altera Stratix V GX* GS = Altera Stratix V GS †	B	Altera Stratix V FPGA Hard IP E = Embedded PCIe*
CC	Altera Stratix V Size A7 = 5SGXA7*	D	Altera Stratix V Transceiver Speed Grade 1 = 14.1 Gbps transceivers † 2 = 12.5 Gbps transceivers † 3 = 8.5 Gbps transceivers*	EE	Altera Stratix V Temperature Range & Speed Grade C2 = Commercial temp. range/speed grade 2 † C3 = Commercial temp. range/speed grade 3* C4 = Commercial temp. range/speed grade 4 †
FF	DDR3 Bank A Size 00 = None A9 = 2 GB (x72)* B9 = 4 GB (x72)† C9 = 8 GB (x72) D9 = 16 GB (x72)†	GG	DDR3 Bank B Size 00 = None A9 = 2 GB (x72)* B9 = 4 GB (x72)† C9 = 8 GB (x72) D9 = 16 GB (x72)†	H	Misc. Configuration 0 = Standard
I	Front Panel Configuration F = FMC Q = QSFP x2	J	Assembly F = Pb-free assembly*		

* Default

† Contact BittWare for availability.

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