

# GX-AMC

## Altera Stratix® II GX AdvancedMC



- High density Altera Stratix II GX supported by BittWare's ATLANTiS™ FrameWork for FPGAs
- BittWare's FINE™ II Host/Control Bridge provides control plane processing and interface
- Front Panel Mezzanine site for I/O and processing expansion
- Over 2 GBytes on-board memory
- I/O includes: 10/100/1000 Ethernet, RS-232, SerDes, LVDS, JTAG

Based on Altera's Stratix II GX FPGA, BittWare's GX-AMC (GXAM) is a mid-size, single wide AdvancedMC that can be attached to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The GXAM features a high-density Altera Stratix II GX FPGA supported by BittWare's ATLANTiS FrameWork, a front panel I/O interface, a control plane interface via BittWare's FINE II Host/Control Bridge, an IPMI system management interface, and a configurable 11x SerDes interface supporting a variety of protocols. It also provides 10/100/1000 Ethernet, two banks of DDR2 SDRAM, and Flash memory for booting the FPGA and FINE.

### Altera Stratix II GX FPGA

At the heart of the GXAM is a state-of-the-art Altera Stratix II GX FPGA which has been specifically designed for serial I/O-based applications and provides up to 19 full-duplex high-performance, multi-gigabit transceivers supporting PCI Express, XAUI, GigE, Serial RapidIO, and SerialLite II standards. It contains up to 132,540 equivalent LEs, over 6.7 Mbits of RAM, 252 embedded 18x18 multipliers, 63 DSP blocks, and 8 PLLs. BittWare's ATLANTiS FrameWork, which enables seamless routing of the I/O, is implemented in the FPGA.

### Fat Pipes, Common Options, and I/O Interfaces

The Altera Stratix II GX interfaces to 3 ports (1, 2, & 3) in the AMC common options region\*, and 8 ports in the AMC fat pipes (4 - 11). These 11 ports provide a network data and control switch

fabric interface on the AMC connector, configurable to support PCI Express, Serial RapidIO, GigE, or XAUI.

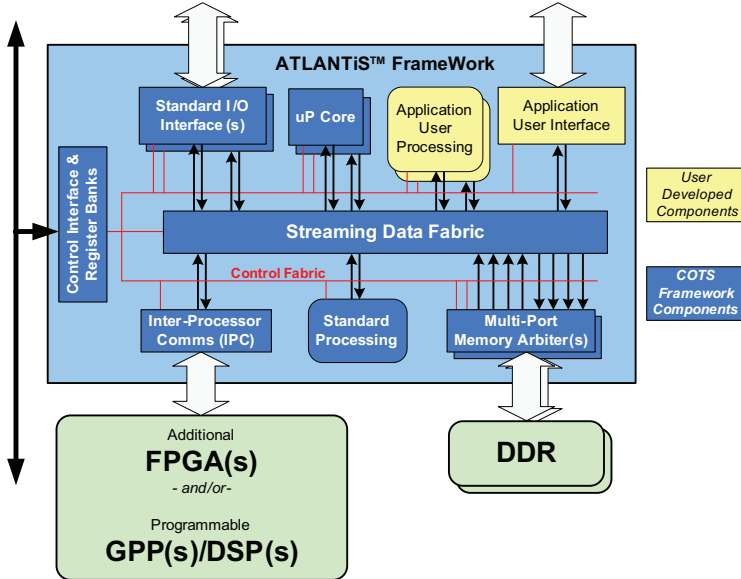
The Stratix II GX provides 4 SerDes and 76 pairs of LVDS I/O to the BittWare front-panel I/O module, and 16 LVDS pairs (8 in, 8 out) are provided for rear panel I/O via the AMC connector (ports 12 - 15, and 17 - 20). All AMC clocks are also connected to the Stratix II GX. The GXAM implements the standard Module Management Control Interface (IPMI).

### ATLANTiS™ FrameWork

BittWare's ATLANTiS FrameWork for FPGA development (see Figure 1) provides reconfigurable FPGA components, along with the infrastructure necessary to implement, simulate, synthesize, validate, and deploy a complete FPGA application on the Stratix II GX. ATLANTiS FrameWork delivers fully validated FPGA physical interfaces for all board-level I/O and communications, including high-speed SerDes and external memory control, along with resource management components such as buffering, DMA engines, and arbitration. Each component can be easily monitored and controlled via an addressed path implemented using Altera's open standard Avalon Memory Mapped Interface. Similarly, Altera's open standard Avalon Streaming Interface is used to implement point to point data transport between ATLANTiS components. A set of reconfigurable fabric components such as multiplexers, switches, decoders, and FIFOs expand the interconnect options for both memory mapped and streaming interfaces. ATLANTiS FrameWork removes the burden of reinventing low-level IP for the FPGA, thus freeing developers to focus on unique value-added development.

\*Only available on the EP2SGX130

Figure 1: ATLANTiS FrameWork Architecture Overview



## FINE™ II Host/Control Bridge

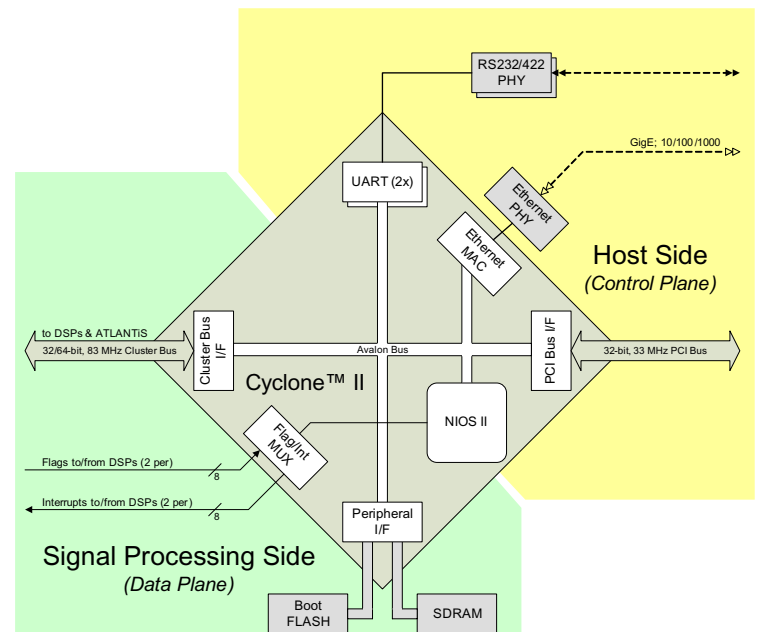
BittWare's FINE II Host/Control Bridge (see Figure 2) implements a complete control plane interface for the GXAM, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. Extensive software support is provided via BittWare's BittWorks Toolkit, which is tightly integrated with the FINE.

The FINE provides GigE via the common options region, along with 10/100 Ethernet and an RS-232 monitor port on the AMC front panel, and is connected to the FPGA via a local control bus.

## Development Tools

BittWare offers complete software support for the GXAM with its BittWorks software tools. BittWorks is a suite of software development tools, designed to make developing and debugging applications for BittWare's signal processing boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely. The BittWorks software tools include host interface libraries, a wide variety of diagnostic utilities and configuration tools, debug tools, and I/O drivers, all of which are tightly integrated with the ATLANTiS FrameWork and the FINE.

Figure 2: FINE II Architecture Overview



## Specifications

### BOARD ARCHITECTURE

#### FPGA

- Altera Stratix II GX (EP2S90/130) supported by BittWare's ATLANTiS™ FrameWork
- Up to 19 full-duplex, high-performance, multi-gigabit SerDes transceivers
- Up to 132,540 equivalent LEs
- Over 6.7 Mbits of RAM
- Up to 63 DSP blocks
- Up to 252 embedded multipliers
- 8 PLLs

#### External Memory

- 2 banks of up to 512 MBytes DDR2 SDRAM configured as x32
- 64 MBytes of Flash memory for booting Stratix II GX and FINE

#### Fat Pipes Interface

- 8 ports (4 - 11) @ up to 3.125 GHz configurable to support PCI Express, Serial RapidIO, GigE and XAUI

#### Common Options Interface

- BittWare FINE™ Host/Control Bridge providing GigE on port 0

- Ports 1, 2 & 3 via ATLANTiS FrameWork, configurable to support PCI Express, Serial RapidIO, GigE, and XAUI\*

#### Other AMC Edge Connections

- All AMC clocks brought to FPGA
- Module Management Control (MMC) Interface implementing IPMI for temperature monitoring and hot-swap support
- 8 ports providing 8 LVDS in and 8 LVDS out

#### AMC Front Panel I/O

- 10/100 Ethernet via FINE
- RS-232 port
- JTAG debug interface to the Stratix II GX †
- 4 SerDes @ up to 3.125 GHz (optional fiber adapter available)

#### BittWare I/O Module Interface

- Supports customizable front-panel I/O
- 76 LVDS pairs (38 in and 38 out)
- Clocks, P/C, JTAG, and DIO signals
- 4 SerDes @ up to 3.125 GHz

#### Size

- AMC mid-size, single width compatible with AMC specification R2.0

### DEVELOPMENT TOOLS

#### BittWorks Tools for Application Development

- BittWorks Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks Porting Kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems
- BWIO - software library for controlling I/O on BittWare boards

#### FPGA and DSP Code Development

- Altera Quartus® II software

#### Development Platforms

- MicroTCA Rapid Development Platform

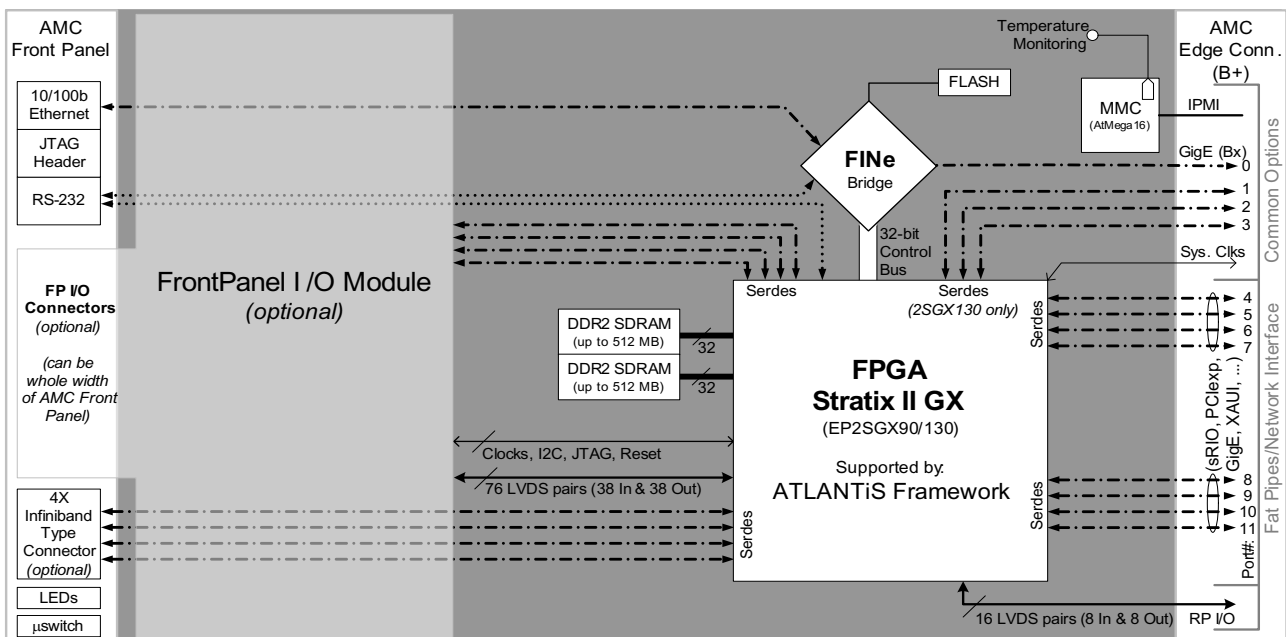
#### Accessory Boards

- BittWare GXBO breakout board for front panel I/O access

\* Only available on the EP2SGX130

† Requires GXBO breakout board

Figure 3: GXAM System Block Diagram



## Ordering Options

### GXAM-RW-AAB-CDE-FGH

RW	Ruggedization 0U = Commercial (0C to 50C)*	AA	FPGA Size 90 = Stratix II GX 90 13 = Stratix II GX 130*	B	FPGA Speed Grade 4 = Commercial Speed Grade 4*	C	Memory Bank 1 0 = None†
D	Memory Bank 2 0 = Not populated 7 = 256 MB DDR2* 8 = 512 MB DDR2†	E	Memory Bank 3 0 = Not populated 7 = 256 MB DDR2* 8 = 512 MB DDR2†	FG	Front Panel Options F1 = Full size, standard outputs	H	Front Panel SerDes 0 = Not populated* 1 = Populated†

\* Default

† Contact BittWare for availability

DS-GXAM | Rev 1.0 | July 2010

© BittWare, Inc. 2010

Stratix II GX and Quartus II are registered trademarks of Altera Corp. All other products are the trademarks or registered trademarks of their respective holders.

**BittWare, Inc.**  
9 Hills Avenue | Concord, NH 03301 USA  
Phone: 603.226.0404  
E-mail: [info@bittware.com](mailto:info@bittware.com)  
[www.bittware.com](http://www.bittware.com)

