

# GT-3U-cPCI

## Ruggedizable Hybrid Signal Processing 3U cPCI Board



- High density Altera Stratix® II GX supported by BittWare's ATLANTiS™ FrameWork for FPGAs
- Four Analog Devices ADSP-TS201S TigerSHARC DSPs
- BittWare's FINE™ II Host/Control Bridge provides control plane processing and interface
- Up to 1 GByte on-board memory
- I/O includes: SerDes, LVDS, RS-232, RS-422, 10/100 Ethernet

**B**ittWare's GT-3U-cPCI (GT3U) is a ruggedized 3U CompactPCI board designed for demanding multi-processor based applications requiring complete flexibility and adaptability. The GT3U features a large Altera Stratix II GX FPGA, one cluster of four ADSP-TS201S TigerSHARC processors from Analog Devices, a front panel interface supplying four channels of high-speed SerDes transceivers, and a back panel interface providing RS-232/RS-422 and 10/100 Ethernet. Simultaneous on-board and off-board data transfers can be achieved at a rate of 2 GB/s via BittWare's ATLANTiS FrameWork, which is implemented in the Stratix II GX FPGA. The board also provides a large amount of on-board memory, including 1 GB of DDR2 SDRAM and 64 MB of flash memory for booting the FPGA and DSPs.

### Altera Stratix II GX FPGA

At the heart of the GT3U is an Altera Stratix II GX FPGA containing 90,960 equivalent LEs, 4.5 Mbits of RAM, 192 embedded 18x18 multipliers, 48 DSP blocks, and 8 PLLs. The FPGA provides pre-, post-, or co-processing to complement the TigerSHARC processing cluster, while also enabling seamless routing of the TigerSHARC I/O at a rate of over 2 GB/s via BittWare's ATLANTiS FrameWork.

### ADSP-TS201S DSPs

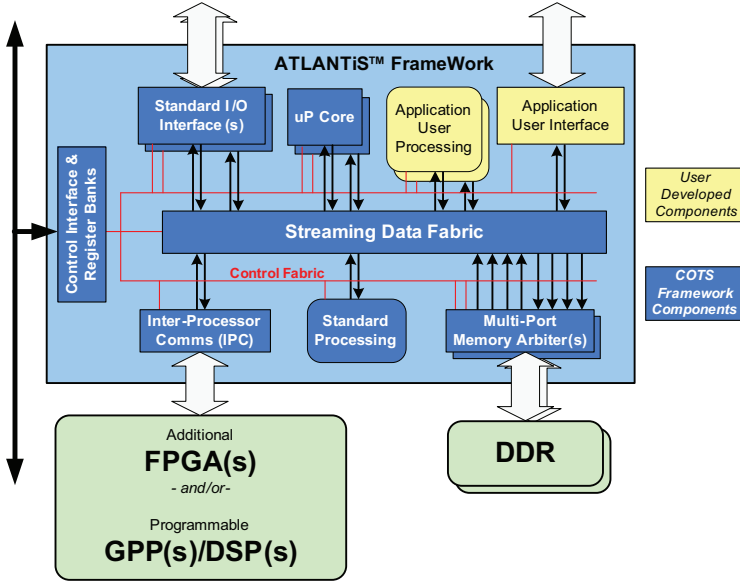
The GT3U features a single cluster of four ADSP-TS201S TigerSHARC DSPs, which are interconnected by a 64-bit cluster bus running at up to 100 MHz. The ADSP-TS201 processor operates at up to 500 MHz, providing 3.0 GFLOPS of peak processing power. Because of its superscalar architecture, the

ADSP-TS201 is also efficient at fixed-point processing, with each DSP supporting 12 BOPS of processing. Along with 24 Mbits of on-chip RAM, each DSP also boasts four high-speed LVDS link ports. Each full-duplex link port is comprised of a 4-bit transmit and a 4-bit receive channel and can support up to 500 MBytes/s in each direction for a total maximum throughput of up to 1 GByte/s. Two link ports from each DSP are used to create an interprocessor communications ring, and the remaining two link ports are routed to the ATLANTiS FrameWork.

### ATLANTiS™ FrameWork

BittWare's ATLANTiS FrameWork for FPGA development (see Figure 1) provides reconfigurable FPGA components, along with the infrastructure necessary to implement, simulate, synthesize, validate, and deploy a complete FPGA application on the Stratix II GX. ATLANTiS FrameWork delivers fully validated FPGA physical interfaces for all board-level I/O and communications, including high-speed SerDes and external memory control, along with resource management components such as buffering, DMA engines, and arbitration. Each component can be easily monitored and controlled via an addressed path implemented using Altera's open standard Avalon Memory Mapped Interface. Similarly, Altera's open standard Avalon Streaming Interface is used to implement point to point data transport between ATLANTiS components. A set of reconfigurable fabric components such as multiplexers, switches, decoders, and FIFOs expand the interconnect options for both memory mapped and streaming interfaces. ATLANTiS FrameWork removes the burden of reinventing low-level IP for the FPGA, thus freeing developers to focus on unique value-added development.

Figure 1: ATLANTiS FrameWork Architecture Overview



## FINe™ II Host/Control Bridge

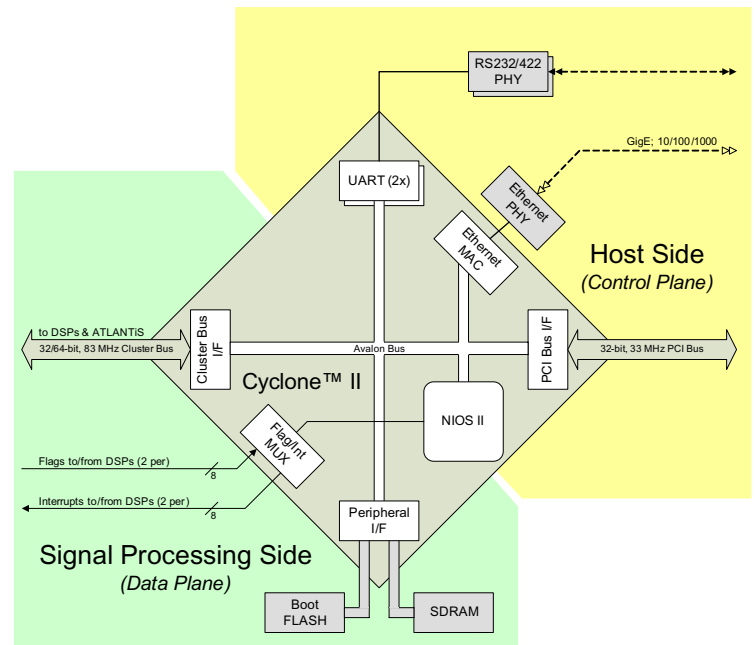
BittWare's FINe II Host/Control Bridge (see Figure 2) implements a complete control plane interface for the GT3U, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. Extensive software support is provided via BittWare's BittWorks Toolkit, which is tightly integrated with the FINe.

The FINe provides the DSPs with low-overhead access to the host via the 32-bit, 33 MHz PCI interface. It also provides a general purpose peripheral bus that allows the DSPs to access the Flash, 10/100 Ethernet, and the RS232/RS422 UART interface. It provides host access to the DSPs, Flash, and FPGA control registers.

## Development Tools

BittWare offers complete software support for the GT3U with its BittWorks software tools. BittWorks is a suite of software development tools, designed to make developing and debugging applications for BittWare's signal processing boards easy and efficient, regardless of whether the hardware is on the local machine or being accessed remotely. The BittWorks software tools include host interface libraries, a wide variety of diagnostic utilities and configuration tools, debug tools, and I/O drivers, all of which are tightly integrated with the ATLANTiS Framework and the FINe.

Figure 2: FINe II Architecture Overview



## Specifications

### BOARD ARCHITECTURE

#### FPGA

- Altera Stratix II GX FPGA supported by BittWare's ATLANTiS™ FrameWork
- Up to 16 full-duplex, high-performance, multi-gigabit transceivers
- Up to 132,540 equivalent LEs
- Up to 78 LVDS channels
- Over 6.7 Mbits of RAM
- Up to 63 DSP blocks, 252 embedded multipliers, and 8 PLLs

#### Processors

- 4 Analog Devices ADSP-TS201S TigerSHARC DSPs
- 500 MHz, 2 ns instruction rate DSP core
- 3 GFLOPS (32-bit floating point) or 12 GOPS (16-bit fixed point) per DSP
- Native support for 32-bit floating point operations and for 8, 16, and 32-bit fixed point operations
- 24 Mbits of on-chip RAM per DSP
- 4 4-bit LVDS link ports at up to 1 GByte/s
- Integrated I/O processor with 14 channel DMA controller

#### External Memory

- 1 GByte DDR2 SDRAM
- 64 MByte Flash memory for booting DSPs and configuring the FPGA

#### BittWare FINE™ Host/Control Bridge

- 32-bit, 33 MHz PCI interface
- GigE and RS-232/422 to rear panel
- Supports host- and Flash-based booting of Stratix II GX FPGAs and ADSP-TS201S
- Runs BittWorks server for full remote access via the BittWorks Toolkit

#### Link Ports

- 8 link ports extend from the ADSP-TS201S DSPs (two per DSP) to the Stratix II GX FPGA
- 8 link ports (two per DSP) dedicated for interprocessor communication
- Each link port runs at up to 1 GByte/s

#### Rear Panel I/O

- BittWare's FINE™ Host/Control Bridge providing 10/100 Ethernet and RS-232/RS-422
- 36 LVDS pairs, 16 inputs and 20 outputs

#### Front Panel I/O

- 4 channels of high-speed SerDes transceivers (available on air-cooled boards only)

#### Size

- 3U single slot (160mm x 100mm)

### DEVELOPMENT TOOLS

#### BittWorks Tools for Application Development

- BittWorks Toolkit - host, command, and debug tools for BittWare hardware
- BittWorks Porting Kit - source code and prebuilt ports for porting the BittWare Toolkit to other operating systems
- BWIO - software library for controlling I/O on BittWare boards

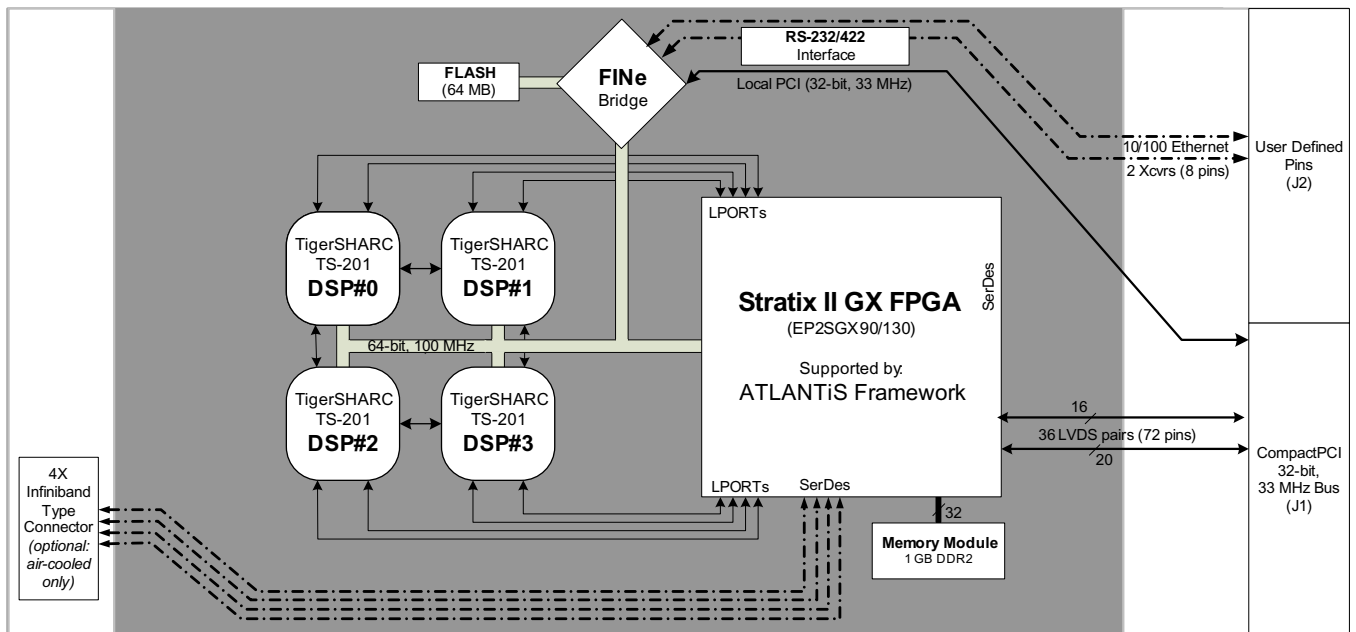
#### FPGA and DSP Code Development

- Analog Devices VisualDSP++
- Altera Quartus® II software

#### Accessory Boards

- BittWare GT3T rear transition module for rear panel I/O breakout

Figure 3: GT3U System Block Diagram



## Ordering Options

GT3U-RW-XZZ-AAB-MMM-CDE					
RW	Ruggedization 0U = Commercial (0C to 50C)* 2C= Conduction cooled; conformal coating (-40C to 75C) † 3C= Conduction cooled; conformal coating (-40C to 85C) †	X	Cluster A DSPs 4 = 4 TS201s DSPs	ZZ	DSP Speed 50 = 500 MHz*
AA	FPGA Size 90 = Stratix II GX 90* 13 = Stratix II GX 130 †	B	FPGA Speed Grade 3 = Speed grade 3 (fastest) † 4 = Speed grade 4* 5 = Speed grade 5 (slowest)	MMM	Memory Module 000 = No memory DO5 = 512 MBytes DDR2* D10 = 1 GByte DDR2
C	SerDes Connector 0 = Not populated * 1 = Populated † (air cooled only)	D	cPCI P2 Connector 0= Not populated 1= Populated*	E	Reference Oscillator 4= 125 MHz*

\* Default

† Contact BittWare for availability.

### GT3U Ruggedization Chart

Characteristics	Commercial	Level 2C	Level 3C**
Type	Air-Cooled	Conduction-cooled	Conduction-cooled
Temperature			
Operating	0°C to 50°C w/ 300 lin.ft/ min airflow	-40°C to 75°C at thermal interface	-40°C to 75°C at thermal interface (w/o memory; limited FPGA power)
Storage	-45°C to 100°C	-55°C to 125°C	-55°C to 125°C
Mechanical			
Vibration	Random; 0.01g <sup>2</sup> /Hz 15Hz to 2kHz	Random; 0.1 g <sup>2</sup> /Hz 15Hz to 2kHz (per MIL-STD-810E)	Random; 0.1 g <sup>2</sup> /Hz 15Hz to 2kHz (per MIL-STD-810E)
Shock	20g peak sawtooth 11 ms duration	30g peak sawtooth 11 ms duration	30g peak sawtooth 11 ms duration
Conformal Coating	No	Yes	Yes
Humidity	0 to 95% non-condensing	0 to 100% condensing	0 to 100% condensing

DS-GT3U | Rev 1.12 | July 2010

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