
Summary:

The ADM-XRC-6TL is a high performance reconfigurable XMC (VITA 42.3 Mezzanine Card) based on the Xilinx® Virtex-6 LXT and SXT ranges of Platform FPGAs.

Features include high speed PCI Express® interface, external memory, high density I/O, temperature monitoring, battery backed encryption and flash boot facilities.

A comprehensive cross platform API with support for Microsoft Windows™, Linux and VxWorks™ provides access to the full functionality of these hardware features.

The optional fitting of the Pn4 connector provides an additional 32 General Purpose IO (GPIO) links to the carrier card.

Features:
Applications:

- Radar/Sonar Beamforming
- ELINT
- Fingerprint Recognition
- Data Encryption

Target Device(s) :

Xilinx Virtex-6 - LX240T, LX365T, LX550T, SX315T, SX475T {FFG1759}

Memory:

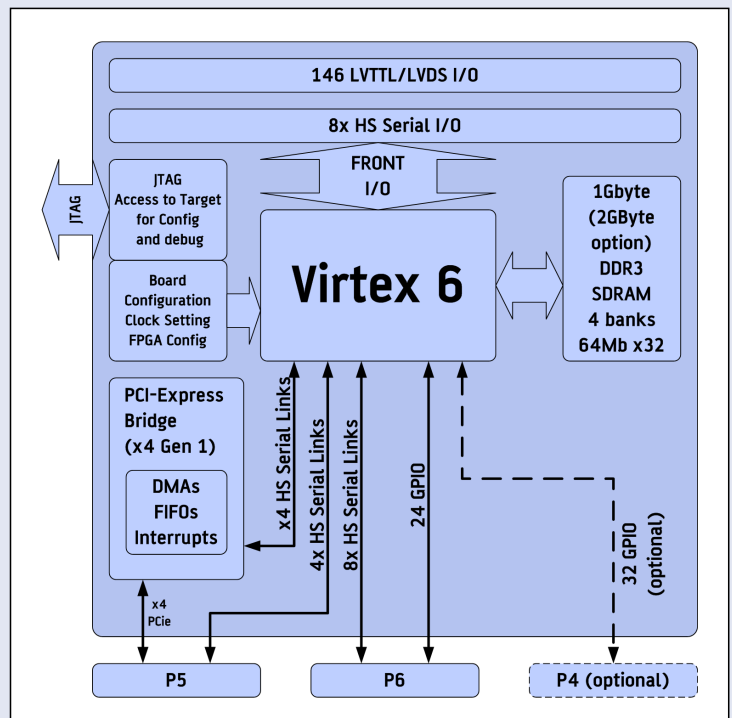
- SDRAM - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s)
- FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.

Front Connector I/O:

- Up to 146 LVCMOS/LVDS I/O. Programmable signaling levels of 1.5V, 1.8V or 2.5V
- 8 High-Speed Serial Links

Rear Connector I/O:

- 8 High-Speed Serial Links via P15 connector (allowing second x4 PCI Express® Gen 2 channel in default mode or single x8 PCI Express® channel in Bridge Bypass mode)
- 8 High-Speed Serial Links via P16 connector (allowing additional PCI Express® Gen 2 channel or user defined protocol)
- 24 GPIO connections via P16 connector (LVTTTL levels)
- 32 I/O connections via optional PMC Pn4 connector (2.5V levels with 3.3V compatible inputs)



Specification

Product Name	ADM-XRC-6TL
Target Device	Xilinx Virtex-6 LX240T, LX365T, LX550T, SX315T, SX475T {FFG1759}
Host I/F	PCI Express x4
Interface	PCI Express® x1, x2, x4 link to separate bridge device with 1GB/s local link to user FPGA 2 DMA Controllers Interrupt Controller
Memory	SDRAM - 1GByte in 4 independent banks (2GByte option) of DDR3 SDRAM @ 800MT/s (32-bit wide so 3.2GB/s) FLASH - Configuration Flash providing an initialisation design for automatic loading into the target FPGA.
Front I/O	Up to 146 LVCMOS/LVDS I/O. Programmable signaling levels of 1.5V, 1.8V or 2.5V 8 High-Speed Serial Links
Rear I/O	8 High-Speed Serial Links via P15 connector (allowing second x4 PCI Express® Gen 2 channel in default mode or single x8 PCI Express® channel in Bridge Bypass mode) 8 High-Speed Serial Links via P16 connector (allowing additional PCI Express® Gen 2 channel or user defined protocol) 24 GPIO connections via P16 connector (LVTTTL levels) 32 I/O connections via optional PMC Pn4 connector (2.5V levels with 3.3V compatible inputs)
Clocks	Low-jitter 125MHz reference clock, suitable for SerDes applications Low-jitter 200MHz reference clock for IOB delay circuits General purpose user clock programmable between 32MHz and 100MHz Custom clock inputs available through the XRM interface
Configuration	PCI Express® direct to SelectMAP port From Flash direct on power up External JTAG connector
Software	Drivers for Microsoft Windows™, Linux and VxWorks™ API with template designs in VHDL
Battery	Battery back-up for IP encryption keys
Environmental	Temperature: Air cooled option Operating Temperature 0° to +55°C Non-Operating(Storage) Temperature -40° to +85°C Operating Humidity 5% to 95% at 40°C non-condensing Non-Operating(Storage) Humidity 5% to 95% at 40°C non-condensing EMC: FCC 47CFR Part 2 EN55022 Equipment Class B

Ordering Codes

ADM-XRC-6TL/z-y(m)(c)(p)

Virtex-6 device	z	LX240T, LX365T, LX550T, SX315T, SX475T
Virtex-6 speed	y	1, 2, 3
Memory Size Fitted	m	blank = 1GByte, /2 = 2GByte
Cooling	c	blank = air cooled commercial, /AC1 = air cooled industrial, /CC1 = conduction cooled industrial
Pn4 Fitted	p	blank = not fitted, /Pn4 = Pn4 Connector fitted
Note	#	not all FPGA speed grades available in all configurations. Contact Alpha Data for full details.