

New!



Features

- Complete software radio interface solution
- VITA 42.0 XMC compatible with switched fabric interfaces
- Four 200 MHz 16-bit A/Ds
- Up to 1.5 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multimodule synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O

General Information

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems.

Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched-fabric interfaces.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The Model 7150 architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters,

DDR2 SDRAM memory, interface FPGA, programmable LVPECLI/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

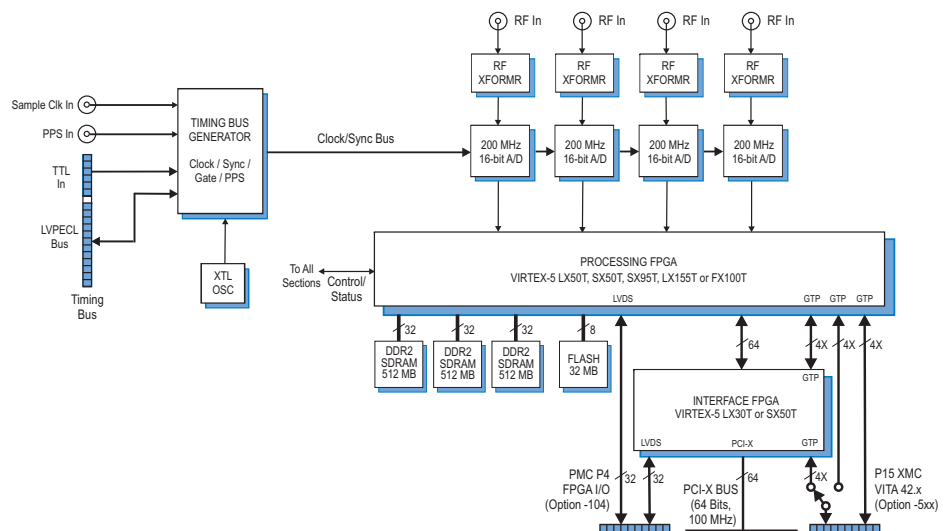
The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7150 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 installs the P4 PMC connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

The Model 7150 architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ▶



XMC Interface

The Model 7150 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides serial data links with up to 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7150 achieves up to 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

► Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules. Up to three slave 7150s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. More modules can be synchronized with an external clock and sync generator.

Memory Resources

Up to three independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7150 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the module. Data widths of 32 or 64 bits and data rates of 33, 66, 100 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, the Model 7150 can be optionally factory-configured with 4X PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Ordering Information

Model	Description
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC
Options:	
-104	FPGA I/O through the P4 connector
-5xx	XMC interface

Contact Pentek for additional available options.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SMC connectors

Transformer Type: Coil Craft WBC1-1TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 250 kHz to 350 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Internal Clock: 200 MHz crystal osc.

External Clock: 10 to 200 MHz

Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock

Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array

Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T

Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O

Available only with SX95T, LX155T and FX100T FPGAs

Option -104: Installs P4 connector with 16 LVDS pairs to the processing FPGA and 16 pairs to the interface FPGA

Memory

DDR2 SDRAM: Up to 1.5 GB in three banks

PCI Interface

PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz

DMA: 4 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C

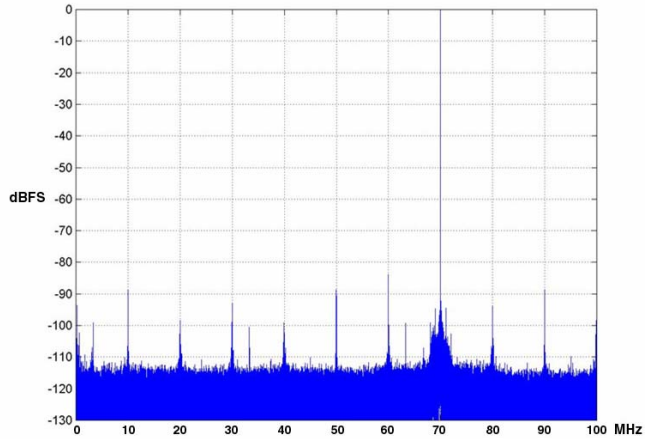
Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

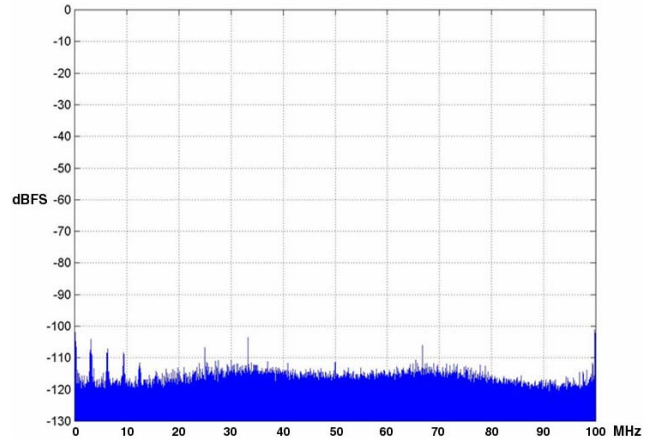
A/D Performance

Spurious-Free Dynamic Range



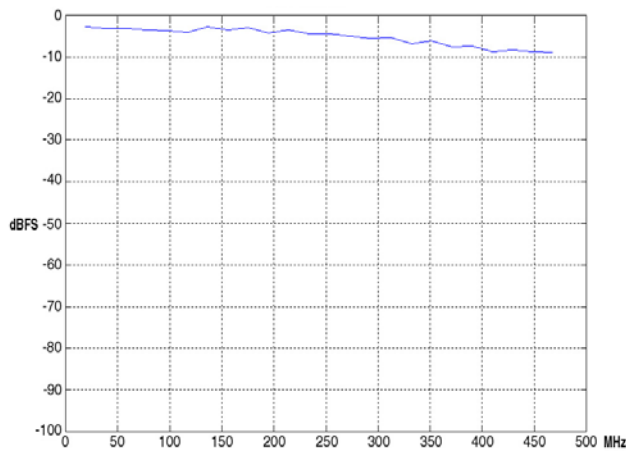
$f_{in} = 70$ MHz, $f_s = 200$ MHz, Internal Clock

Spurious Pickup



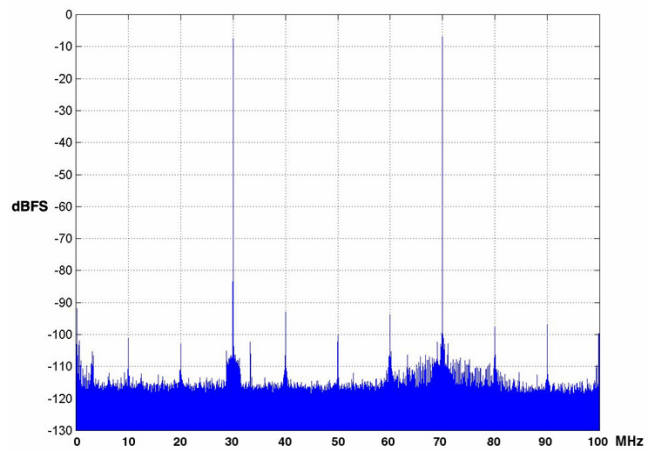
$f_s = 200$ MHz, Internal Clock

Input Frequency Response



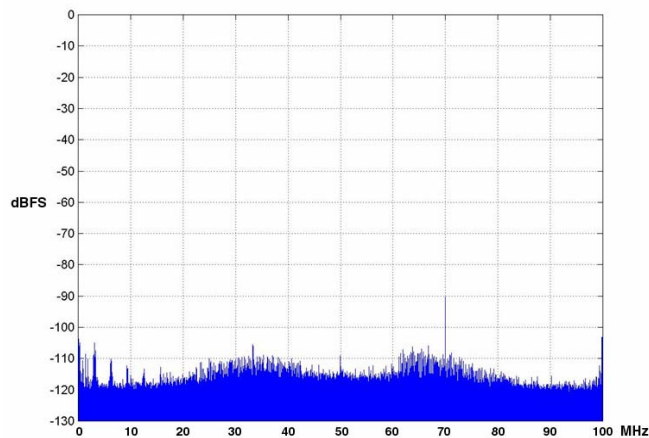
$f_s = 200$ MHz, Int. Clock

Two-Tone SFDR



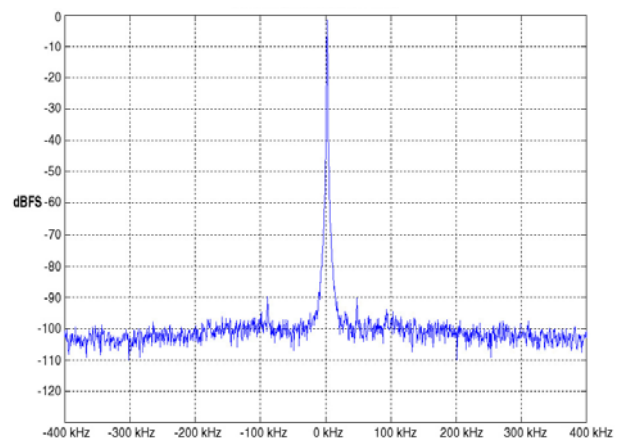
$f_{in1} = 30$ MHz, $f_{in2} = 70$ MHz, $f_s = 200$ MHz, Int. Clock

Adjacent Channel Crosstalk



$f_{in} = 70$ MHz, $A_{in} = 0$ dBFS, $f_s = 200$ MHz, Int. Clock

Phase Noise at 70 MHz



$f_s = 200$ MHz, Int. Clock