

What does the IP-EP200-EDK Engineering Design Kit contain?

The IP-EP2 Series Engineering Design Kit (EDK) includes a variety of files to assist the user in their development of the IP-EP2 Series Module. A summary of the various components of the EDK is given below.

- **NineK528a.vhd:** Top-Level Acromag provided VHDL (hardware design language) source file. Supports IP bus interface to ID, INT, and IO space.
- **Clkgenc.vhdl:** Acromag provided VHDL source file. Supports the programming of the Cypress Clock IC.
- **GID_IO_8.vhd:** Acromag provided VHDL source file. Supports 8 channels of digital change of state (COS) interrupts.
- **NineK528a.qsf:** Quartus II assignments file. This ASCII file contains all required user assignments included FPGA pin assignments and device options.
- **NineK528a.pof:** Altera specific configuration file. This file is generated by the Quartus II software and is used to directly program the FPGA via JTAG.
- **NineK528a.jic:** Altera specific configuration file. This file is generated by the Quartus II software and is used to program the FLASH device via JTAG.
- **NineK528a.hex:** Hexadecimal (Intel-Format) configuration file. The Hex file is an ASCII file in the Intel Hex format. This file is generated by the Quartus II software and is used to direct program the FPGA over the IP bus.
- **NineK528a.qpf:** Altera Quartus II specific master project file. Use to file to open the Quartus II example design project provided on the CD.

In addition to the VHDL design files, the IP-EP2 Series Engineering Design Kit includes a schematic, parts list, parts location drawing, manuals, and other utility programs.

- **4502063a.pdf:** IP-EP2 Series Schematic and Part Location Drawing
- **IPEP2_797a.pdf:** IP-EP2 Series User's Manual
- **IPEP2_Programming_Guide.pdf:** IP-EP2 Series Engineering Design Kit Programming Guide.
- **IPEP201.pdf:** Part list for IP-EP201(E) model.
- **IPEP202.pdf:** Part list for IP-EP202(E) model.
- **IPEP203.pdf:** Part list for IP-EP203(E) model.
- **IPEP204.pdf:** Part list for IP-EP204(E) model.
- **HFileGenerator.exe:** This program generates 'C' style .h output file from an Intel.hex input file such as the NineK528a.hex file. The .h file can be used to "compile in" the Altera configuration data into your own C program. This program can also be modified to allow programming of the IP-EP2 Series module over the IP bus. However you will need the base address of the IP-EP2 module in your system.
- **HFileGenerator.c:** Source C file for HfileGenerator.exe
- **BitCalc2k1.exe:** The BitCalc2k1.exe file is an executable program which provides the register values needed to program the clock generator chip. By entering the desired frequency, and selecting the IP clock speed (8MHz or 32MHz), this program will compute the correct values to write to the Clock control Registers.
- **IPEP2_Assignments.xls:** Summary of Quartus II assignments in excel format. The pin assignments can be copied directly into Quartus II.